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# THESIS

MICROPROCESSOR CONTROLLED
INSTRUMENTATION/NAVIGATION PACKAGE
FOR HOSTILE MARINE ENVIRONMENTS

by

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**Currently, many shipboard instrumentation systems are inoperative or inaccurate when AC power is lost to the bus supplying power to the instrumentation. Instrumentation is also subject to failure when it comes into contact with water during a flooding, fire, or steamline rupture casualty. A small, inexpensive, standardized instrumentation package that is water resistant and capable of being powered from a standby battery power source is needed. This research is directed toward developing such an instrumentation system. To prove the water resistance of the system it was first installed on a windsurfing craft. Water resistant sensors using readily available components were also developed in this project.**

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Microprocessor Controlled Instrumentation/Navigation
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## ABSTRACT

Currently, many shipboard instrumentation systems are inoperative or inaccurate when AC power is lost to the bus supplying power to the instrumentation. Instrumentation is also subject to failure when it comes into contact with water during a flooding, fire, or steamline rupture casualty. A small, inexpensive, standardized instrumentation package that is water resistant and capable of being powered from a standby battery power source is needed. This research is directed toward developing such an instrumentation system. To prove the water resistance of the system, it was first installed on a windsurfing craft. Water resistant sensors using readily available components were also developed in this project.

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# I. INTRODUCTION/PROBLEM STATEMENT

## A. GENERAL

Shipboard electronic instrumentation systems in use today have many drawbacks. They are inoperative or inaccurate when the AC bus supplying power to the instrument is lost. Electronic instruments may fail when exposed to water from flooding casualties, from firehoses during firefighting, or from water vapor during a steam header rupture casualty. With a large number of electronic instruments installed, the power consumed by instrumentation may become a significant load on the ship's electric plant. Instrumentation that consumes significant power also becomes a heat load that must be counteracted by the ship's air conditioning and other cooling systems.

A microprocessor based, battery powered, water resistant instrumentation package is one possible answer to the above mentioned problems. The instrumentation package should be easily adaptable to many different sensors. This would allow many instruments throughout the ship to use similar packages. Parts inventories could thus be reduced since all instruments would be the same basic design and use the same basic parts.

Training shipboard personnel about all the different instrumentation onboard could be more efficient if a standardized package were used. Technicians could spend more time learning the intricacies of a basic system and be more effective at maintaining and troubleshooting instrumentation.

Storage of data collected would also be useful to shipboard personnel. As an example, personnel operating a nuclear power plant could use this data to diagnose conditions of the plant during and following a casualty.

The sensors used should be low power, water resistant, and accurate. The instrumentation package should be able to quickly process the information supplied by the sensors and display the data.

## B. WINDSURFING APPLICATION

To prove the design, the package is intended to be tested on a windsurfing craft with 5 water resistant sensors. This provides the opportunity to test the package in a salt water environment under high shock conditions. It also gives a case where the sensor inputs can be used to evaluate performance of a real situation.

Information that would be useful for evaluating windsurfing performance is as follows:

- board speed across the water
- true wind speed
- wind direction relative to the board

- sail sheeting angle
- fin angle of attack
- efficiency (board speed/wind speed)
- velocity made good (speed going upwind or downwind)
- max speed
- average speed
- distance traveled
- elapsed time

To be useful for performance evaluation, the package must be able to download the data it has collected so that the data can be evaluated on a computer.

## II. COMPONENT SELECTION

### A. GENERAL

Component selection was the first step in the design. In order to meet the low power requirement, complimentary metal oxide semiconductor (CMOS), digital components were required. To make the system perform at a high rate, high speed CMOS (HC family) components were used.

### B. MICROPROCESSOR SELECTION

The component around which the instrumentation package is built is the microprocessor. To start the design, a microprocessor needed to be chosen. A high speed CMOS microprocessor was the first component selected. The Motorola MC68HC11E0 eight-bit microcontroller was chosen. A copy of the pinout is available in Figure A1 of Appendix A [Ref. 1].

The MC68HC11E0 (HC11E0) is an 8-bit high speed CMOS microcontroller that is readily available and inexpensive. The HC11E0 has 5 ports built onto the chip to make it easy to interface other devices to the microcontroller without a lot of external interface chips [Ref. 2]. This makes the HC11E0 ideal for use in an instrumentation system. Ports include an address and data bus, an 8 channel analog to digital converter, an asynchronous serial communications interface, a synchronous serial communications interface, a 16-bit free

running timer system, and an 8-bit pulse accumulator. The chip has low power consumption and allowable clock rates that range from static to 3 MHz. The HC11E0 also possesses a power saving feature that can be used to retain data during a low voltage condition. A diagram showing the input/output structure is included as Figure A2 of Appendix A [Ref. 1].

The HC11E0 has 512 bytes of RAM on chip. In addition to RAM, other versions in the 68HC11 family of microcontrollers have maskable ROM, EPROM, and EEPROM on chip. All versions of the chip use the same instruction set so that software developed using one version of the chip will run on other versions with slight modification. A table of the different versions of the 68HC11 available is included as Figure A3 of Appendix A [Ref.2].

The 68HC11 family has two major modes of operation, single-chip mode and expanded mode [Ref. 2]. Single-chip mode is used when the program that the microcontroller is running is stored on the microcontroller during manufacture in the form of ROM. Single-chip mode is not useable on the HC11E0 since the mask ROM is not available on this chip (this is set at the factory by the value stored in an EEPROM register referred to as CONFIG). Expanded mode allows the microcontroller to operate an external address and data bus with 64 kilobytes of addresses available. It should be noted that internal RAM and internal registers appear in this 64 kilobytes with on-chip addresses having priority over off-chip

addresses. There are also two special modes available, special bootstrap and special test. Special bootstrap is available for single-chip mode, while special test is available for expanded mode. Special modes can be used for testing a system for proper operation. The mode of operation is determined by the external levels applied to 2 pins on the HC11E0, MODA and MODB.

The differing models of the 68HC11 family share the same programmers model [Ref. 2]. The model consists of two 8-bit accumulators, A and B. The accumulators may be combined into one 16-bit accumulator, referred to as accumulator D. Two 16-bit address registers, X and Y, are included. A 16-bit stack pointer (SP) register is provided for stack manipulation. A 16-bit program counter (PC) is provided to keep track of the next instruction to be used. An 8-bit condition code register is used to store flags set by instructions. A drawing of the programmer's model is included as figure A4 of Appendix A [Ref. 2].

## C. DISPLAY SELECTION

A display was needed to show collected data and real time calculations to the user. In order to meet the low power requirement, LCD technology was chosen. The Optrex DMC 40218 is a 40 character by 2 line LCD display with integral CMOS drivers on the unit [Ref. 3]. This display was chosen as it

was inexpensive, readily available, and advertized as easy to interface to microprocessors.

### D. PROGRAM STORAGE

CMOS based EPROM was chosen to store system programs in order to make the instrumentation package easy to reconfigure, as necessary, for different applications. The 27C64 is an 8 kilobyte by 8-bit CMOS EPROM that is inexpensive, readily available from several different manufacturers, and has the same storage capacity as the ROM available on the base model of the 68HC11 family, the MC68HC11A8 [Ref 4]. This was the chip chosen to hold programs in the instrumentation package.

### E. DATA STORAGE

Static RAM was needed to store data collected. CMOS should be specified if the package is put into production, but was unavailable for the prototype described in this thesis. ALP static RAM was used as a substitute, which has pinouts and operation similar to available CMOS RAM. The Hyundai 62256ALP-70 was an economical and available option and was thus chosen for the prototype [Ref. 5].

### F. COMBINATIONAL LOGIC

Altera EPLDs were chosen for combinational logic as they are CMOS, use low power, are easily programmed with equipment available in the digital lab, save board space, and can be reused [Refs. 6,7].

## G. SENSORS

For the windsurfing application, sensors needed to be chosen. All of the sensors needed to be water resistant. Since the whole package was to be battery powered, all sensors should use little power. Each sensor should be light in weight, so as to have as little effect on windsurfer performance as possible. Since the sensors will be located external to the basic package, it was decided that a digital output from each sensor would be preferred to minimize the effects of the connecting wires on accuracy. To be able to calculate all of the parameters listed for the windsurfing application detailed in chapter I, five sensors are needed. The sensors are:

- board speed
- fin angle of attack
- sail sheeting angle
- wind direction relative to the sail
- apparent wind speed

Commercially available sensors for windspeed and angle measure were not found that would meet the requirements of this application. Units available are in general not water resistant. The windspeed indicators, in general, give an analog output through a small fixed magnet generator driven by a tricup assembly. Wind angle sensors are generally constructed using a 2 pole rotating magnetic field with a

number of taps driven by an attached wind vane. Both of the devices are heavy, not water resistant, and give analog output [Ref. 8].

### 1. BOARD SPEED

For board speed through the water, a commercially available unit was sought. A paddlewheel unit was chosen that is similar to what was used by Winner [Ref. 9]. The unit, an Interphase TI-0200-016, was obtained through a marine retailer. The paddlewheel has 5 vanes, one of which has an internal magnet, attached to a rotating drum. A Hall effect sensor is placed near the vanes path in the housing. As the vane with the internal magnet approaches the Hall effect sensor, the magnetic flux causes the sensor to switch on, giving a positive pulse until the magnet moves away from the sensor. Thus, one complete rotation of the paddlewheel gives five pulses. A thermistor is also enclosed on the housing in order to sense water temperature. This could easily be tied into one of the analog to digital converter channels on the HC11E0 to demonstrate how analog signals could be used by the package [Ref. 10].

### 2. WIND SPEED

To build a light and water resistant windspeed sensor, a solid state photodarlington transistor was chosen. These devices are cheap, light, and readily available. To trigger the photodarlington, an opaque cylinder with a slot exposed to

ambient light, coupled to a standard tricup assembly, was developed [Ref. 11].

## 3. ANGULAR MEASUREMENT

To measure the three angles for the windsurfing application, optical encoders were selected. An optical encoder is a device that gives off a 2-bit digital compatible gray code as the shaft of the device is rotated. By noting the last 2 gray code bits and the present 2 gray code bits, the direction of rotation in known. The optical encoder is available in a number of resolutions and sizes. Bourns ENS1JB28L00256 type optical encoders [Ref. 12] were chosen as these are small, light, and have a resolution of 256 gray code transitions, which interfaces easily into an 8-bit microprocessor (note $2^8 = 256$). These devices were not available in a water resistant form so a method of making them water resistant was devised.

# III. PACKAGE DESIGN

## A. DESIGN OVERVIEW

The basic aim of the instrumentation package design is to use the HC11E0 in the expanded mode to collect, store, and display any data gathered by the sensors. As a starting point, the M68HC11 Reference Manual [Ref. 2] provides a diagram of suggested basic expanded mode connections. This basic design was then modified to suit this particular application. A hierarchial schematic of the instrumentation package is provided in Appendix B. An explanation of the connections follows.

## B. CONNECTIONS TO THE MICROPROCESSOR

Vdd, pin 26, is wired to +5 volts and Vss, pin 1, is wired to ground as the sole power supplies to the HC11E0. Three capacitors (10, 1, 0.01 uF) are connected from Vdd to ground to provide for power supply bypassing of switching transients for the HC11E0 [Ref. 2]. The +5 volts is generated by 6 AA alkaline cells connected through a switch to a MC78M05B positive 5 volt regulator [Ref. 13].

To set expanded mode on the HC11E0, MODA and MODB must be driven high. Both are connected to +5 volts via a 4.7 kohm resistor [Ref. 2]. A normally open switch connected between MODB and ground allows the package to enter special test mode

if desired. Note that during operation, the MODA pin also doubles as a load instruction register (LIR) indicator, thus necessitating the pull-up resistor. LIR can be used during system debugging to show when the HC11E0 is fetching a new instruction into the instruction register.

To generate the clock of the HC11E0, an external AT cut crystal is connected in parallel with a 10 Mohm resistor across XTAL and EXTAL. The crystal frequency used is 4 times the external clock desired (e.g., an 8 MHz crystal is used to generate a 2 MHz external clock). Both EXTAL and XTAL are connected to ground via 18 pF capacitors. These capacitors should be as closely matched as possible to provide for accuracy of the clock. For actual layout on a PCB, all of these leads should be kept as short as possible [Ref. 2].

In expanded mode, all of the 68HC11 family uses a multiplexed address and data bus. During a read or write, the address is first output to pins 9-16 (lower order bits) and to pins 35-42 (higher order bits). Address strobe (AS) is also asserted at this time. In order to keep the lower byte of the address available on the address bus during a read or write cycle, an 8-bit octal latch (74HC373) is used [Ref. 2]. The latch is hardwired with the output enable (OE) always asserted. AS from the HC11E0 is used to latch a new valid address on to the address bus by connecting directly to the latch enable on the 74HC373 [Ref. 14]. The outputs of the 74HC373 drive the lower order byte of the address bus. The

upper order byte of the address bus is driven directly from pins 35-42, which are dedicated solely to this purpose in expanded mode. After AS is negated, the data appears directly on the data bus which is hardwired directly to pins 9-16. Delays in the combinational logic that generates the output enable signals for devices connected to the data bus is sufficient to prevent any contention between the lower address byte and the data on the data bus. All 8 lines of the data bus are connected to ground via 10 kohm pull-down resistors [Ref. 2].

The RESET pin on the HC11E0, when asserted low, places the HC11E0 into reset. This causes the HC11E0 to retrieve the reset vector which is stored in memory at hexadecimal address FFFE-FFFF. The RESET pin is also used to indicate an internal failure of the HC11E0. The pin is an open drain output during program execution. For this reason, the RESET pin may not be directly connected to a pull-up resistor and a switch to ground, as this may result in corruption of EEPROM registers in the HC11E0, including the important CONFIG register [Ref. 2]. The recommendation of the M68HC11 Reference manual has been followed, and the RESET pin has been connected to a 4.7 kohm pull-up resistor, an MC34064 [Ref. 15] low voltage inhibit circuit, and to an MC34164 [Ref. 16] low voltage inhibit circuit [Ref. 2]. The MC34064 input pin (IN) is connected to the +5 volt power supply and the ground pin (GND) to ground. The open drain output of the MC34064 drives RESET

low until 4.6 volts is sensed between the input and ground connections. The input of the MC34064 is connected to a 4.7 kohm pull-up resistor, a 1 uF capacitor connected to ground, and to a 4.7 kohm resistor connected to ground in series with a normally open switch. When power is applied to the pull-up resistor on the MC34164, it also holds it's open drain low until 4.3 volts are sensed between IN and GND. The devices have different voltage inhibit values to prevent contention. During operation, the HC11E0 may be reset simply by pressing the normally open switch connected to the MC34164.

The XIRQ and IRQ pins may be used by devices external to the HC11E0 to trigger an interrupt. Both pins are connected to 4.7 kohm pull-up resistors. If a need arises to use interrupts for an application, an open drain source for each interrupt may be connected to either pin [Ref. 2]. Each interrupt source should have an interlock circuit to keep asserting the interrupt pin when multiple requests for interrupt are received and the HC11E0 finishes processing an interrupt. Several registers control operation of these pins which are described in the M68HC11 Reference manual. A copy of the registers list is provided in Appendix C [Ref 1]. For the windsurfing application, interrupts on these pins were not used.

The pins associated with Port D, pins 20-25, on the HC11E0 are multifunctional. The value written to several registers selects the function of the pins. They may be configured as

general purpose, bidirectional, input/output pins. Pin 20(PD0/Rxd) and pin 21 (PD1/Txd) may be configured as dedicated receive and transmit pins, respectively, for the Serial Communications Interface (SCI) [Ref. 2]. For the instrumentation package, these pins are connected to a circuit that can be connected to a serial port of another computer. This allows the instrumentation package to download, or receive data from, another computer. The remaining four pins of PORT D may be configured as a Serial Peripheral Interface (SPI). The SPI is not used in the windsurfing application, and thus pins 22-25 are connected to 10 kohm pull-up resistors. The function of all of the PORT D pins are controlled by setting values in registers of the HC11E0.

The pins associated with PORT A, pins 27-34, on the HC11E0 make up another multifunctional port. The function of the pins is selected by writing values into associated registers. Three of the pins can be used only for input. Four pins may only be used for output. The final pin may be configured as an input or output pin. PORT A includes a timer system for the HC11E0. The three input-only pins may function as timer input capture (IC) pins, while the four output-only pins may be used as timer output compare (OC) pins. The last pin may be used as a general input/output pin, as another output compare pin, or as the input to a pulse-accumulator circuit [Ref. 2]. For the windsurfing application, the windspeed sensor pulse train is connected to pin 32, IC1. The board

speed through water paddlewheel sensor output is connected to pin 33, IC2. All other pins are connected to 10 kohm pull-up resistors for the windsurfing application.

The pins associated with PORT E, pins 43-50, on the HC11E0 may be used as general purpose input only pins, or as 8 separate inputs to an analog to digital converter. The function of the pins is again selected by writing values to associated registers [Ref. 2]. For the windsurfing application, pin 43 is connected to the output of the thermistor from the paddlewheel sensor. This allows the thermistor to sense water temperature. All other pins are connected to pull-up resistors.

The last two remaining pins on the HC11E0 are pin 51, voltage reference low (VRL), and pin 52, voltage reference high (VRH). Voltages on these pins set the high and low voltages for the analog to digital converter system. For the windsurfing application, VRH is connected to +5 volts via a 1 kohm resistor. VRL is connected directly to ground. A 1 uF capacitor is connected between VRH and VRL to provide a bypass path [Ref. 2].

### C. MEMORY MAP

Memory locations for all components needed to be specified. The control registers in the instrumentation package were located at the beginning of the memory map. The

memory locations for all other components and registers are detailed in Appendix D.

## D. PROGRAM STORAGE

To store the programs for the HC11E0, a 27C64 EPROM was used. Pins for address (A0-A12) on the 27C64 are connected to the 13 lowest order address bits. The data pins (DQ0-DQ7) are connected to appropriate lines on the data bus. VCC and VPP are connected to +5 volts, with a 0.1 uF bypass capacitor connected from VCC to ground. GND is connected to ground. OE and CE are connected to output pins on an EP310, which is configured to generate the necessary signals. The design of the EPLD is detailed in Appendix E. PGM and NC remain unconnected. Note that the 27C64 appears in the memory map at locations E000-FFFF hexadecimal.

## E. EXTERNAL DATA STORAGE

Two HY62256ALP 32-kilobyte by 8-bit static RAM chips are connected to the address and data busses, with the exception of A15 which has no pin on the RAM chips. The CS inputs to each chip are generated by the output of two pins on an EPLD. OE and WE are common to both chips and are also generated by an EPLD detailed in Appendix E. VCC is connected to +5 volts and GND to ground. The two RAM chips have address space that does not appear in the memory map of the instrumentation package. The lower order RAM covers addresses 0210-0FFF

hexadecimal. The higher order RAM covers addresses 1000-DFFF hexadecimal.

## F. DISPLAY

The last component to be integrated into the basic package design was the display. The DMC 40218 LCD display uses 8 data bits (DB0-DB7), an external clock signal (E), a read/write input (R/W), and a register select input (RS). A summary of the commands used to control the DMC 40218 is included as Appendix F [Ref. 3].

RS provided a challenge to the design as the HC11E0 provided no convenient output to drive RS while operating in the expanded mode. It was decided to give the display two consecutive addresses in order to generate the RS input externally. For reading or writing data to and from the display registers, address 0200 hexadecimal was used. Address 0201 hexadecimal was used to allow the data bus to write or read control codes for the display. The RS input to the DMC 40218 is generated when address 0200 hexadecimal is on the data bus. As the final package was to run with a clock speed of 2 MHz, the clock supplied to the display needed to be reduced to a maximum of 1 MHz. The E, RS, and R/W inputs to the display are generated using an EP310 EPLD that is detailed in Appendix G.

To prevent contention on the data bus, the display is connected to two 74HC373 octal tristate latches. One latch is

activated on a write to hold the data for the display, while the other is to latch data read from the display to the data bus. The logic for enabling and latching the tristate latches is implemented in an EP310 detailed in Appendix G.

# IV. SENSOR DESIGN

In order to implement the package for the windsurfing application, 5 sensors are needed as a minimum. These are board speed through the water, fin angle of attack, sail sheeting angle, relative wind with respect to the sail, and apparent wind speed.

## A. BOARD SPEED

The board speed through the water is needed to measure the distance the board travels in a certain amount of time. It was decided to use a product already available from the maritime industry. This device is a TM-0200-016 paddlewheel transducer made by Interphase. The device consists of a paddlewheel with 5 vanes on a drum that rotates. Internal to each vane is a magnet. The housing has a Hall effect switch that has been sealed. When the paddlewheel is forced to rotate by passage across the water, the changing magnetic field caused by the magnets causes the Hall effect switch to turn on and off for each passage of a vane. The power required is a standard digital +5 volts. This output is connected directly to an input capture pin on the HC11E0 timer system (PORT A).

The output of the transducer is a square wave pulse train with digital levels. As an added feature, a water resistant thermistor is also included in the transducer housing. The thermistor is connected to one channel of the analog to digital converter system (PORT E) on the HC11E0 and a pull-up resistor. The other side is connected to ground. This allows for measurement of water temperature. Although water temperature is not required for the windsurfing application, it was decided to add the feature since it was available for free.

The paddlewheel transducer is mounted on an aluminum T bar assembly that extends behind the board. The paddlewheel is offset to the port (left) side of the centerline of the board. This places the paddlewheel out of the turbulence caused by the fin of the board. Figure H1 of Appendix H shows the transducer.

## B. ANGULAR MEASUREMENT

### 1. OPTICAL ENCODERS

All three of the angle measuring devices use optical encoders with a resolution of 256 positions per rotation. The optical encoder output is a 2-bit Gray code. In a clockwise rotation, outputs B and A change in an incremental manner [e.g., (B,A) 0,0 - 0,1 - 1,1 - 1,0 - 0,0 ]. For rotation in the counterclockwise direction, the gray code transitions in

the opposite order [e.g., (B,A) 0,0 - 1,0 - 1,1 - 0,1 - 0,0].

**2. DIRECTION OF ROTATION**

By observation of the bit stream, the direction of rotation can be easily detected by simply noting the previous position and the current position. As an example, assume that at the start the B and A outputs are 0,0. The shaft is rotated until a change in the outputs of the encoder is noted. If the outputs of the encoder are now 0,1 then rotation was in the clockwise direction. If the outputs of the encoder changed to 1,0 then rotation was in the counter clockwise direction.

**3. INTERFACE TO DATA BUS**

The Gray code output of the encoders could possibly be connected into the interrupt structure of the HC11E0, but since most of the interrupt pins will only recognize either a high to low or low to high transition, half of the angular resolution of the encoders would be lost. In addition, external logic would also be required to generate separate clockwise and counter-clockwise interrupts for each encoder. It would also cause a large number of interrupts on the package during directional changes of the board. It was decided that polling would work best for the angular measurements.

### *a. POSITION KEEPING*

In order to efficiently poll memory when angular data is needed, an external circuit that keeps track of position was required. Two 74HC191 binary up/down counters were connected together to provide an 8-bit representation of the encoder's angular position [Ref. 17]. The 74HC191 counters required two inputs to count up or down. The inputs needed are a clock pulse (CLK), which positive edge triggers the 74HC191 to count one position, and a DN/UP input to determine the direction that the 74HC191 will count. The load and preselect bits can be used to initialize the counter to a known initial position.

### *b. FINITE STATE MACHINE*

To generate the CLK and DN/UP inputs from the Gray code output of the encoder, an asynchronous finite state machine (FSM) was needed. The FSM takes the last known position of the gray code and compares it with what is being currently received from the encoder. If the previous Gray code and the current Gray codes differ, then the CLK (COUNT) supplied to the 74HC191 goes low. Next, DN/UP is changed if needed. The previous Gray code stored is updated to the new code. Finally, the CLK input to the 74HC191 counter is brought high, causing the counter to increment or decrement by one. The method of implementing the FSM asynchronously, presented in Wakerly [Ref. 18], was followed to generate

excitation equations for the FSM. To actually build the FSM, an EP320 EPLD was used. Each FSM uses two input pins and four output pins of the EP320, thus allowing the FSMs for two separate encoders to be built on one EP320, thus saving on the number of components used. Details of the FSM designs are included as Appendices I and J.

### *c. BUS INTERFACE*

To interface the output of the counters to the data bus, one 74HC373 octal latch is used. When the memory location of the angle desired is addressed on the data bus, the decoding logic asserts the LD input to the latch and enables the OE input of the latch delivering the data to the data bus.

### *d. WATER RESISTANT DESIGN*

Each encoder needed to be made water resistant. Encasing the encoder in marine-grade epoxy sealed all of the encoder with the exception of the shaft. A seal chamber was devised that was threaded to match the threads on the shaft guide of the encoder [Ref. 19]. The opposite end of the seal chamber is bored to fit an oil seal for the quarter-inch diameter shaft of the encoder. After an appropriate oil seal is pressed into the chamber, the chamber is screwed onto the shaft guide of the encoder sealing the threads with a silicone sealant. The oil seal needs to be lubricated with boat trailer bearing grease to reduce friction and extend the life

of the oil seal wiper. Details of the seal chamber are drawn in Appendix K. Electrical connections need to be sealed with silicone sealant following soldering of leads.

**4. FIN ANGLE OF ATTACK**

For fin angle of attack, the encoder will be coupled to a trailing fin mounted on the T-bar assembly on the opposite arm of the paddlewheel. As the angle of attack of the fin changes, the trailing fin changes it's angle relative to the center of the board, thus driving the encoder to a new position. The trailing fin is offset from the centerline of the board. This was done to minimize the effects of turbulence generated by the skeg of the board on the trailing fin.

**5. SAIL SHEETING ANGLE**

Sail sheeting angle is measured from a single end of the universal joint connecting the sail and mast to the board. The side of the universal joint that was opposite the encoder needed to be modified in order to prevent inaccuracy in sail sheeting angle measurement [Ref. 19]. This was done by machining a new spud that has parallel channels on either side. The parallel channels are engaged by two parallel rods that engage the channels of the spud to a housing connected to the mast track of the board. The encoder is driven by a socket that fits onto the head of a bolt that connects the universal joint to a mast extension adapter cup. The encoder

is locked inside the mast extension adapter cup by a retaining pin, and is kept tight in the cup by use of foam tape [Ref. 19]. An external clamp to attach the mast extension to the mast extension adapter cup was also fabricated. The typical internal spring pin assembly was removed from the cup to make room for the sail sheeting angle encoder. Drawings of the devised parts are included in Appendix K.

### 6. WIND ANGLE RELATIVE TO SAIL

A wind vane fabricated from divinycell, fiberglass, epoxy, and aluminum rod was constructed. The vane is directly coupled to an optical encoder, which in turn is mounted on an aluminum extension in front of the mast. The extension attaches directly to the mast with Velcro straps. The extension is angled so that when the sail rakes back towards the tail of the board in normal sailing position, the wind vane is parallel to the water. Alignment of the wind vane and extension are critical to accuracy of the sensor and any deviation will cause errors in the data acquired.

## C. WIND SPEED

The last sensor is for the apparent wind speed. A standard tri-cup assembly is mounted on a shaft. A cylindrical shroud to exclude light is then directly coupled to the tri-cup assembly. A single hole was cut into the shroud. A photodarlington transistor pair was mounted on a divinycell washer such that light is occluded from the

transistor, with the exception of the one hole in the cylindrical shroud. The photodarlington is connected electrically to +5 volts through a 500 ohm resistor and a potentiometer. The apparent wind causes the tri-cup assembly to rotate the cylindrical shroud. As the shroud rotates, the light reaching the photodarlington varies, causing it to alternately conduct (in light) and cutoff (in darkness). The output is the voltage across the photodarlington. It was anticipated that ambient light would be sufficient to cause a square wave output to be generated that could be used to drive one of the input capture channels on the HC11E0. The apparent wind speed sensor is mounted on the same vertical axis underneath the wind vane on the same aluminum extension.

### D. WIND SENSOR EXTENSION POSITION

The extension needed to be far enough in front of the sail to minimize localized variations in wind speed and direction generated by the sail. After conversations with Matthew Avila, aeronautical engineer, and Trevor Baylis, owner/designer of Waddel Sails, it was decided that as a minimum, the wind speed and direction sensors needed to be one quarter of the chord length of the sail, upstream. The chord length used should be the horizontal distance from the sails leading edge to the trailing edge at the attachment point for the aluminum wind sensor extension. The extension length is 2 feet between the wind sensors and the mast.

# V. IMPLEMENTATION

To implement the design, software and hardware were developed. The hardware consisted of building a wire wrap prototype of the instrumentation package to support the windsurfing application. Software was developed to test the wire wrap prototype board.

## A. SERIAL ADDITION OF COMPONENTS

The intent for testing the design was to first write a short program to output a message to the display unit on the wire wrap prototype. After the display was shown to be working properly, additional components would be added and tested one by one. This way, any problems caused by adding one component would be found easily if the package worked properly prior to adding that component. Once the wire wrap prototype worked properly, the components would be placed on a custom printed circuit board. The finished printed circuit board was to be long and slender to fit inside a sealed section of PVC pipe, and carried inside the mast extension of a windsurfing craft.

## B. TEST PROGRAM

Software for the prototype was developed using an assembler and simulator from Pseudo Corporation [Ref.21]. The

"Hello" program that was written was successfully simulated when the simulator was configured like the wire wrap prototype. A copy of the "hello" program is included as Appendix K.

The "hello" program was loaded onto an AM27C64 EPROM. This proved to be a major stumbling block as the 29B Universal Programmer in the digital lab on campus was not up to date. The AMD part used was not covered in the documentation, and thus it was necessary to try the algorithms for other manufacturer's devices. A few AM27C64s were damaged during this process. A family code that programmed the device was finally found. However, the programming yields of the devices were unacceptable. An average of two program/erase cycles per device, prior to the device failing, was obtained. This problem has plagued testing efforts.

## C. SENSOR IMPLEMENTATION

The sensors have all been fabricated for the windsurfing application. The mounts are all custom made from common aluminum extrusions available at hardware stores.

### 1. BOARD SPEED AND FIN ANGLE OF ATTACK

The board speed paddlewheel transducer and the fin angle of attack are mounted on a T-bar assembly fabricated from aluminum. The T-bar assembly connects to the board via the fin retaining screws of a standard Tuttle fin box. To increase resolution of the fin angle of attack, timing gears

were attached to the shafts of both the trailing fin and the fin angle of attack encoder. The gear ratios used were 80 teeth on the trailing fin shaft and 40 teeth on the fin angle of attack encoder shaft. A miniature timing belt connects the gears of the two shafts. This gives a ratio of 2:1 between the trailing fin and the fin angle of attack encoder. This ratio gives the angle of attack encoder a resolution of approximately 0.7 degrees vice the 1.4 degrees if the encoder was directly driven by the trailing fin. The sine/cosine table of this encoder is also different from the other two encoders. The shaft for the trailing fin is fit to precision thrust and axial bearings to reduce friction in the shaft. A picture of the T-bar mount is included in Appendix H.

**2. WIND SPEED**

The wind speed sensor was fabricated from a custom made three-sixteenths inch stainless steel shaft. Two precision axial needle bearings were press fit into a larger plastic housing to receive the shaft. The shaft is retained in position in the plastic housing by set screw collars on the shaft at the points where the shaft exits the plastic housing. To reduce friction between the collars and the plastic housing, stainless steel precision thrust bearings are placed between the collars and the plastic housing. The tri-cup rotor assembly is connected to the end of the shaft by a retaining screw that goes through the center of rotation of

the tri-cup assembly and into a hole threaded in the end of the shaft. Inside the shroud, the photodarlington is mounted on a divinycell washer and sealed with epoxy.

### 3. RELATIVE WIND ANGLE

The relative wind angle encoder shaft is coupled to a custom wind vane with a set screw collar that is epoxied to the wind vane. The wind vane was fabricated using a symmetrically foiled divinycell fin that was covered by 4 ounce E-glass type fiberglass and West marine epoxy. The fin was glued to a 2 foot aluminum rod. To balance the rod, stainless steel nuts were threaded on the end of the rod opposite the fin.

The wind speed and wind direction sensors are mounted on an aluminum extension that is retained by two velcro straps around the mast. The wind direction sensor is mounted above the wind speed sensor on the same vertical axis at the end of the extension. Two horizontal slits were made in the leading edge of the sail at a height of 9 feet from the tack (the bottom most part of the sail). The material at the slit was then folded behind the mast when the mast is inserted into the sail. This allows the extension to be free of the sail when the sail rotates around the mast. The ends of the extension that contact the mast were then covered with a liquid plastic used to make tool grips. This was done to provide more

friction to prevent movement of the extension. Photographs of the mounted sensors are include in Appendix H.

**4. SAIL SHEETING ANGLE**

The sail sheeting angle sensor was mounted in the mast extension adapter cup. The socket that drives the encoder shaft is coupled directly to the encoder shaft using set screws fit into the end of the socket. When the sail and mast rotate together, the mast extension adapter cup moves relative to a bolt that attaches the adapter cup to a fixed universal joint. This relative motion is what the encoder is actually measuring. Pictures of the sensor are included in Appendix H.

**5. SENSOR CONNECTION**

Water resistant cables and connectors will be needed to connect the sensors to the instrumentation package. These have not been acquired yet.

# VI. TESTING AND EVALUATION

## A. WIRE WRAP PROTOTYPE

### 1. IMPROPER OPERATION

The wire wrap prototype is currently not operating properly. Initially, obtaining the low voltage inhibit circuits required for the design, proved to be difficult. Running the prototype without the low voltage inhibit circuits installed, may allow the EEPROM based CONFIG register to be corrupted during power up of the HC11E0. It is believed that this is what has happened to the prototype, although this has not been verified as the source of failure on the prototype. To complicate matters, failures of the AM27C64 EPROMs have frequently been experienced.

### 2. TROUBLESHOOTING

Connecting the prototype to a regulated current limiting power supply and to a logic analyzer, it was observed that the HC11E0 microcontroller was operating, but not executing the instructions that were contained in the external AM27C64 EPROM. When RESET was asserted, the reset vector was addressed at location FFFE-FFFF hexadecimal. Next, it was shown that the starting location of the "HELLO" program was loaded onto the data bus as the vector E000 hexadecimal (the

address location of the start of the program stored in the EPROM) using the logic analyzer.

The E clock output of the HC11E0 was measured with an oscilloscope and found to be 2 MHz with an 8 MHz crystal installed, and 1 MHz with a 4 MHz crystal installed. The AS output of the HC11E0 was also observed to be present using an oscilloscope.

During testing, the "HELLO" program did not ever access either of the addresses of the display. The decoding EPLDs were tested on a logic lab, and found to be implementing the correct logic functions. Therefore, the problem appeared to be in either the HC11E0 itself, or in the program. The "HELLO" program was then simulated successfully using a PseudoMax cross-simulator configured like the prototype. This indicates that the problem is either with the HC11E0 itself, or a wiring error on the prototype. Photographs of the pertinent logic analyzer and oscilloscope traces are included in Appendix M.

## B. SENSOR EVALUATION

The sensors have all been tested electrically. The tests were conducted using a regulated power supply set at +5 volts.

The paddlewheel output was measured using an oscilloscope. As the paddlewheel was turned, a square wave output was observed. A picture of the oscilloscope trace is included in Appendix N.

The wind speed sensor was tested using a digital voltmeter to measure the output. Testing showed that the output, under a best case scenario for ambient light, varied from 0.7 volts to 4.3 volts. To provide a better output for the instrumentation package, an adjustable trigger level Schmitt Trigger, such as the MC14583B, is needed [Ref. 22]. The Schmitt Trigger has yet to be acquired and tested, but it should provide adequate levels for the package.

The optical encoder circuit was built on a breadboard and analyzed using a logic lab. This test showed that the circuit operated properly for both clockwise and counter clockwise rotation of the encoder. A photograph of the testing apparatus is included in Appendix O.

Further testing of the sensors will have to wait until the instrumentation package is running properly. When this occurs, the sensors will all be connected to the package and then tested on the water.

## VII. FUTURE DEVELOPMENTS

Future development for this instrumentation system is wide open. The most pressing problem is to successfully troubleshoot the wire wrap prototype. Once the wire wrap prototype is operational, connection of the sensors to the instrumentation package will need to be accomplished. The display and the instrumentation package will require water resistant enclosures that have yet to be fabricated.

To make the water resistant encoder more useful for low torque applications, another seal is needed. The oil seals used (i.e., CR 2560) provide too much friction for the wind angle sensor to operate properly in light wind situations.

The serial communications feature of the instrumentation package needs to be built and tested. This will allow for the package to be more useful for a variety of applications.

To realize the potential for the windsurfing application, a GPS receiver could be integrated into the instrumentation package along with a small compass. With the data collected from the 5 sensors developed, a GPS receiver,and a compass, position fixing capability and evaluation of drift and current are possible. In this configuration, the package could provide enough information for long distance travel of any marine craft. This may allow for use of sail craft and

personal water craft (i.e., a Jet Ski) as covert insertion vehicles [Ref. 23].

To further study phenomena associated with sailing, several other sensors have been conceived that could prove to be useful. A lower drag wind sensor could be constructed by attaching a pitot tube to a small differential pressure cell integrated into a wind vane. This would offer a lower wind drag than the tri-cup windspeed rotor. A lower drag windspeed instrument may allow for placement of several wind instruments at different heights to measure the wind gradient on a sail. A control system could then be built to align the twist (i.e. the difference in rotational angles of the sail about the mast at different sail heights) of the sail to maximize performance for the measured wind gradient.

A differential pressure cell connected to orifices on either side of the fin may give good data on fin performance. This would allow for a scientific evaluation of the fin design instead of the subjective evaluation used today.

To allow for greater reliability in shipboard applications, a method of determining position of an optical encoder following a loss of power to its circuitry is needed. The position of an optical encoder is lost if power to the encoder or its associated circuitry is lost and then restored. This is a disadvantage of the optical encoder when it is driven, for example, by a pressure bellows. The analog

pressure detectors do not lose their calibration when power is removed from them.

To reduce the number of chips and hopefully the power required to use an optical encoder, a single chip interface chip needs to be developed. This chip development is being pursued as a project at the Naval Postgraduate School in the VLSI design class (EC4870).

# VIII. CONCLUSIONS

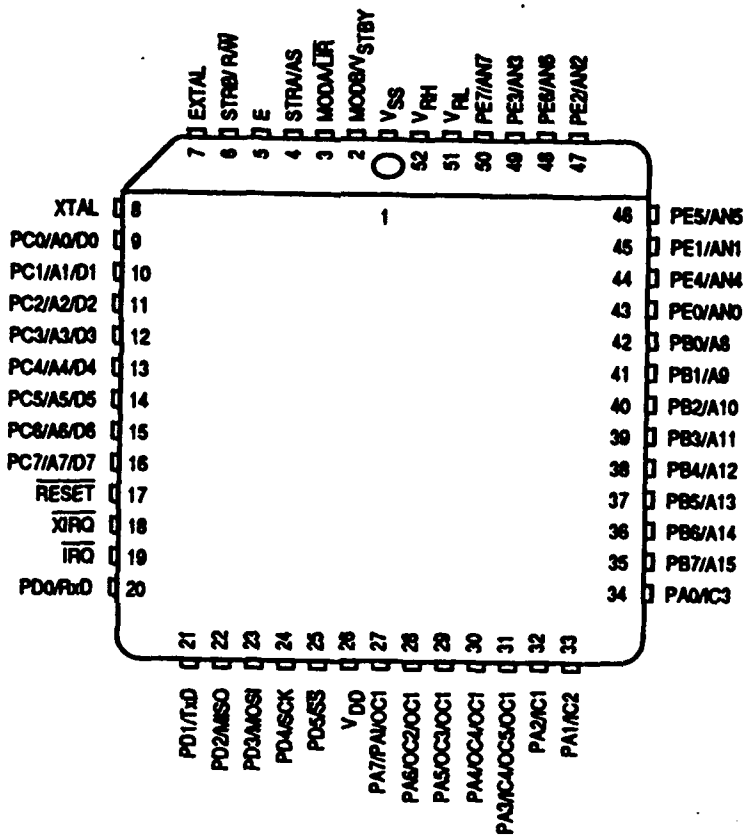
The concept of a simple universal instrumentation package is feasible. With some more work and added expertise, the package designed in this thesis will work.

Using the optical encoder in a microprocessor based system has been shown to be easily accomplished using off the shelf components. Development of a single chip interface for the optical encoder may provide an even better method of integrating optical encoders into systems.

The optically driven wind speed sensor may provide a lighter and lower cost alternative to the generator type of sensors now in use. A lower drag pitot tube design may prove to be better yet.

Knowledge gained by physically implementing system hardware is an extremely useful aspect that is sometimes neglected in engineering education. The experience gained in this thesis would not have been gained through software simulation of circuitry alone. It is much more difficult to design a system when you actually have to purchase the components and pay for the components with your own money. The component research phase is a lengthy and sometimes frustrating process.

# APPENDIX A: MOTOROLA MC68HC11E0




**52-Pin PLCC Pin Assignments**

FIGURE A1

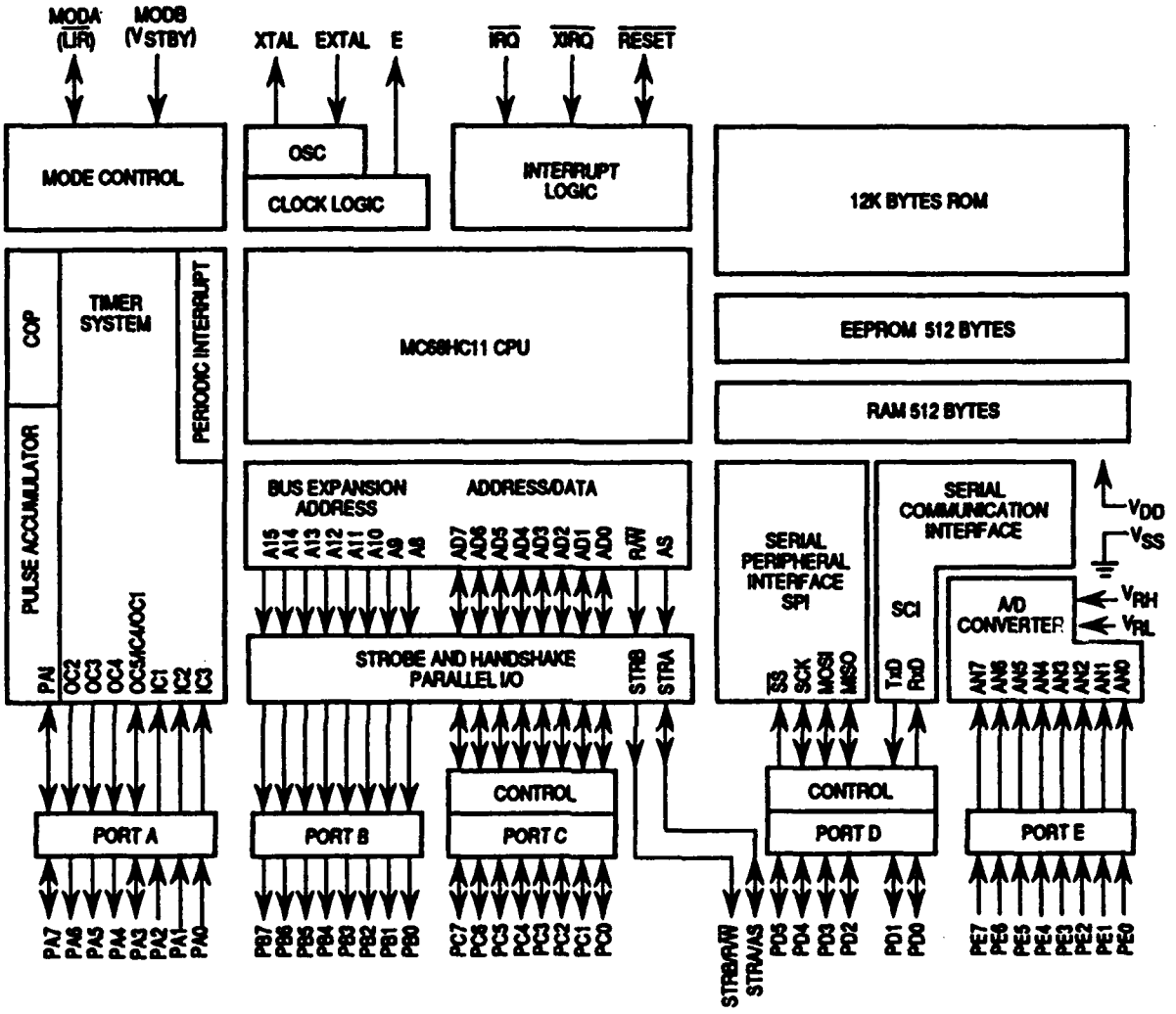

MODA (LIR)
MODB (VSTBY)
XTAL
EXTAL
E
IRQ
XIRQ
RESET
MODE CONTROL
OSC
CLOCK LOGIC
INTERRUPT LOGIC
12K BYTES ROM
COP
TIMER SYSTEM
PERIODIC INTERRUPT
PULSE ACCUMULATOR
MC68HC11 CPU
EEPROM 512 BYTES
RAM 512 BYTES
BUS EXPANSION ADDRESS
ADDRESS/DATA
A15 A14 A13 A12 A11 A10 A9 A8
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
R/W
AS
SERIAL PERIPHERAL INTERFACE SPI
SERIAL COMMUNICATION INTERFACE
SCI
A/D CONVERTER
VDD
VSS
VRH
VRL
PAI OC2 OC3 OC4 OC5/IC4/OC1 IC1 IC2 IC3
STROBE AND HANDSHAKE PARALLEL I/O
STRB
STRA
SS SCK MOSI MISO
TxD RxD
AN7 AN6 AN5 AN4 AN3 AN2 AN1 AN0
CONTROL
PORT A
PORT B
PORT C
CONTROL
PORT D
PORT E
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0
PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0
PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0
STRB/R/W
STRA/AS
PD5 PD4 PD3 PD2
PD1 PD0
PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0

FIGURE A2

**Table 1-1. M68HC11 Family Members**

| Part Number | EPROM | ROM | EEPROM | RAM | CONFIG[2] | Comments |
|---|---|---|---|---|---|---|
| MC68HC11A8 | — | | 512 | 256 | $0F | Family Built Around This Device |
| MC68HC11A1 | — | — | 512 | 256 | $0D | 'A8 with ROM Disabled |
| MC68HC11A0 | — | — | — | 256 | $0C | 'A8 with ROM and EEPROM Disabled |
| MC68HC11A2 | — | — | 2K[1] | 256 | $FF | No ROM Part for Expanded Systems |
| MC68HC811A8 | — | — | 8K + 512 | 256 | $0F | EEPROM Emulator for 'A8 |
| MC68HC11E9 | — | 12K | 512 | 512 | $0F | Four Input Capture/Bigger RAM/12K ROM |
| MC68HC11E1 | — | — | 512 | 512 | $0D | 'E9 with ROM Disabled |
| MC68HC11E0 | — | — | — | 512 | $0C | 'E9 with ROM and EEPROM Disabled |
| MC68HC11E2 | — | — | 2K[1] | 256 | $FF | Like 'A2 with 'E9 Timer |
| MC68HC11D3 | — | 4K | — | 192 | N/A | Low-Cost 40-Pin Version |
| MC68HC711D3 | 4K | — | — | 192 | N/A | One-Time-Programmable Version of 'D3 |
| MC68HC11F1 | — | — | 512[1] | 1K | $FF | High-Performance, Nonmultiplexed 68-Pin |

NOTES:
1. The EEPROM is relocatable to the top of any 4K memory page. Relocation is done with the upper four bits of the CONFIG register.
2. CONFIG register values in this table reflect the value programmed prior to shipment from Motorola.

FIGURE A3 M68HC11 FAMILY MEMBERS

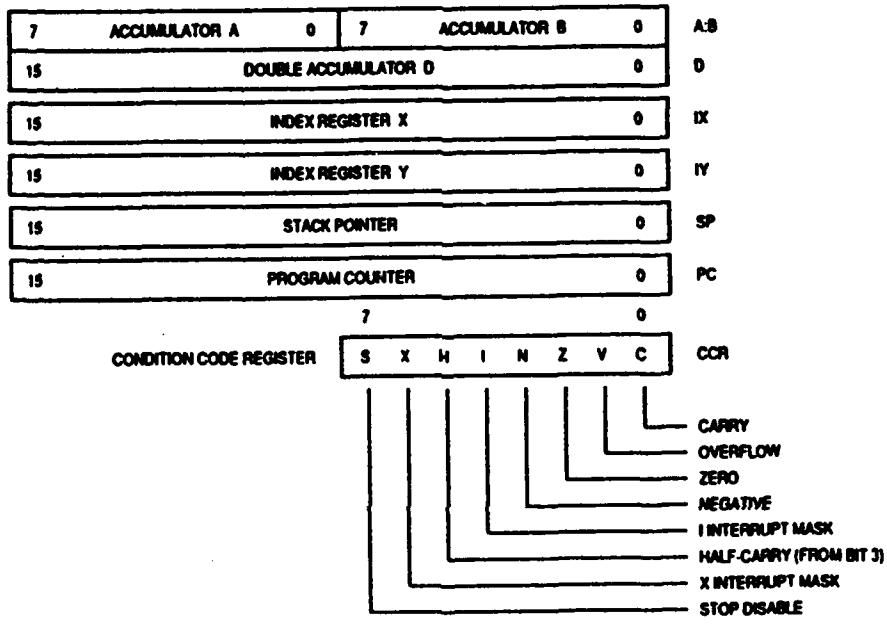
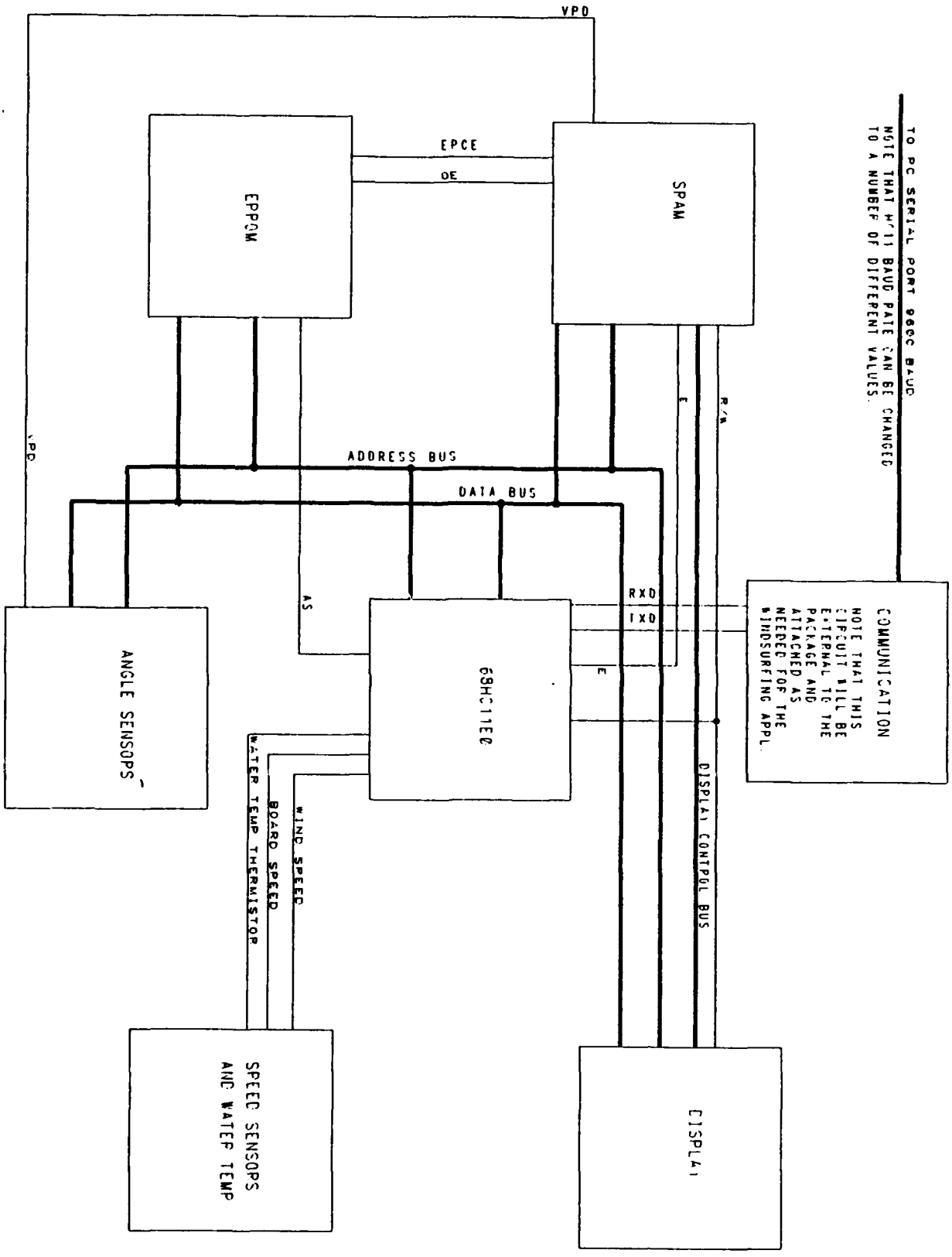


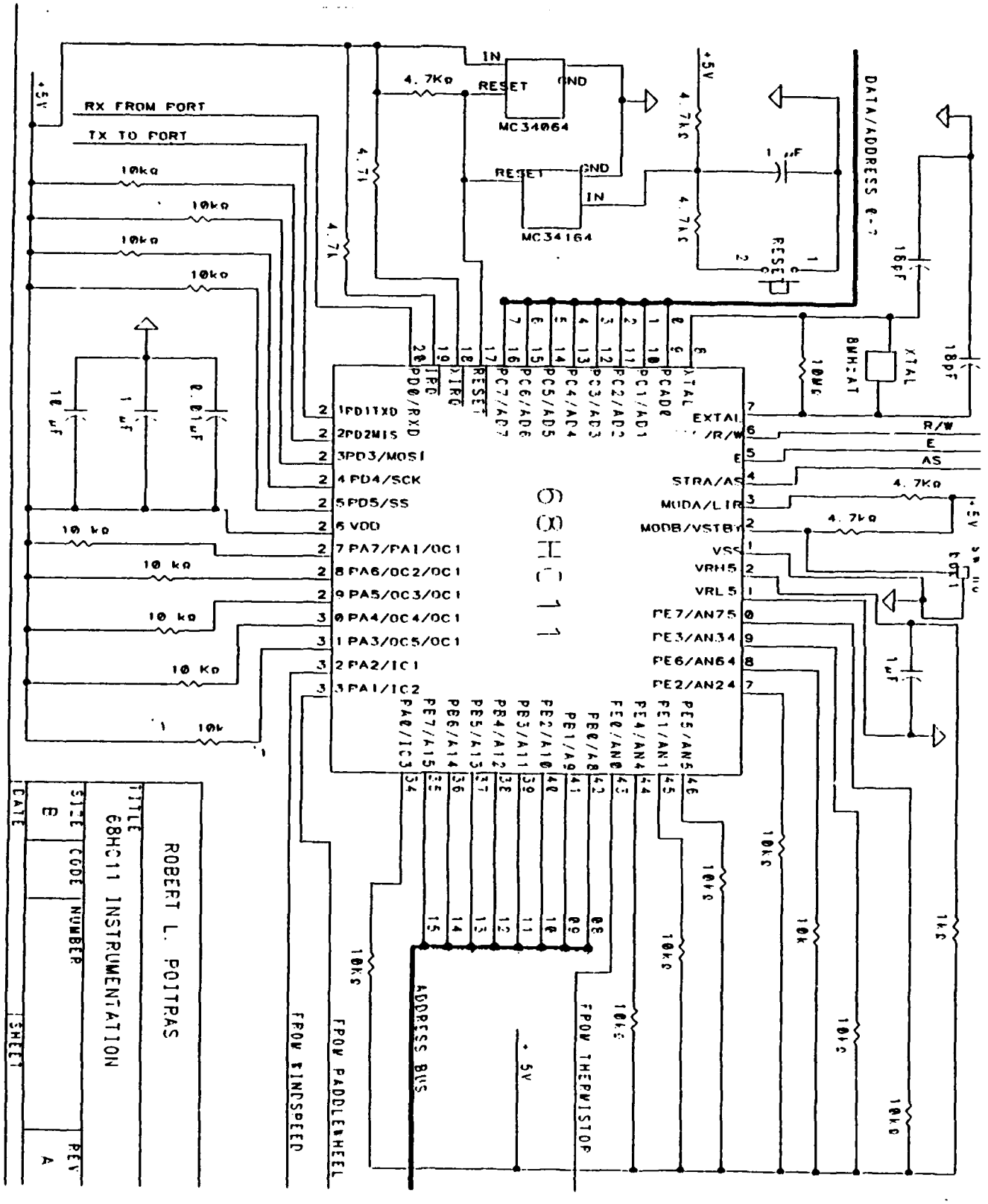

**Figure 1-2. M68HC11 Programmer's Model**

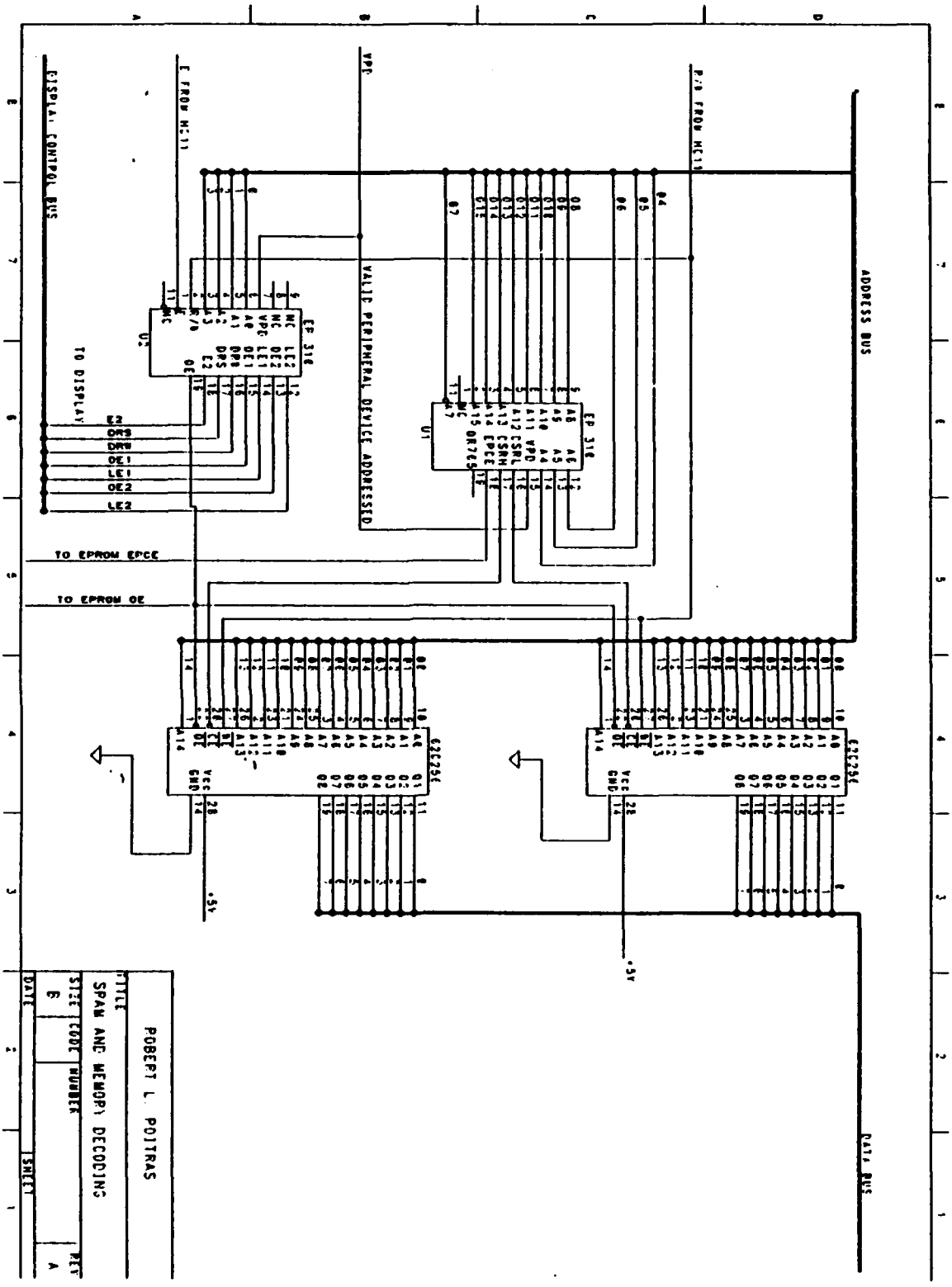
FIGURE A4 M68HC11 PROGRAMMER'S MODEL

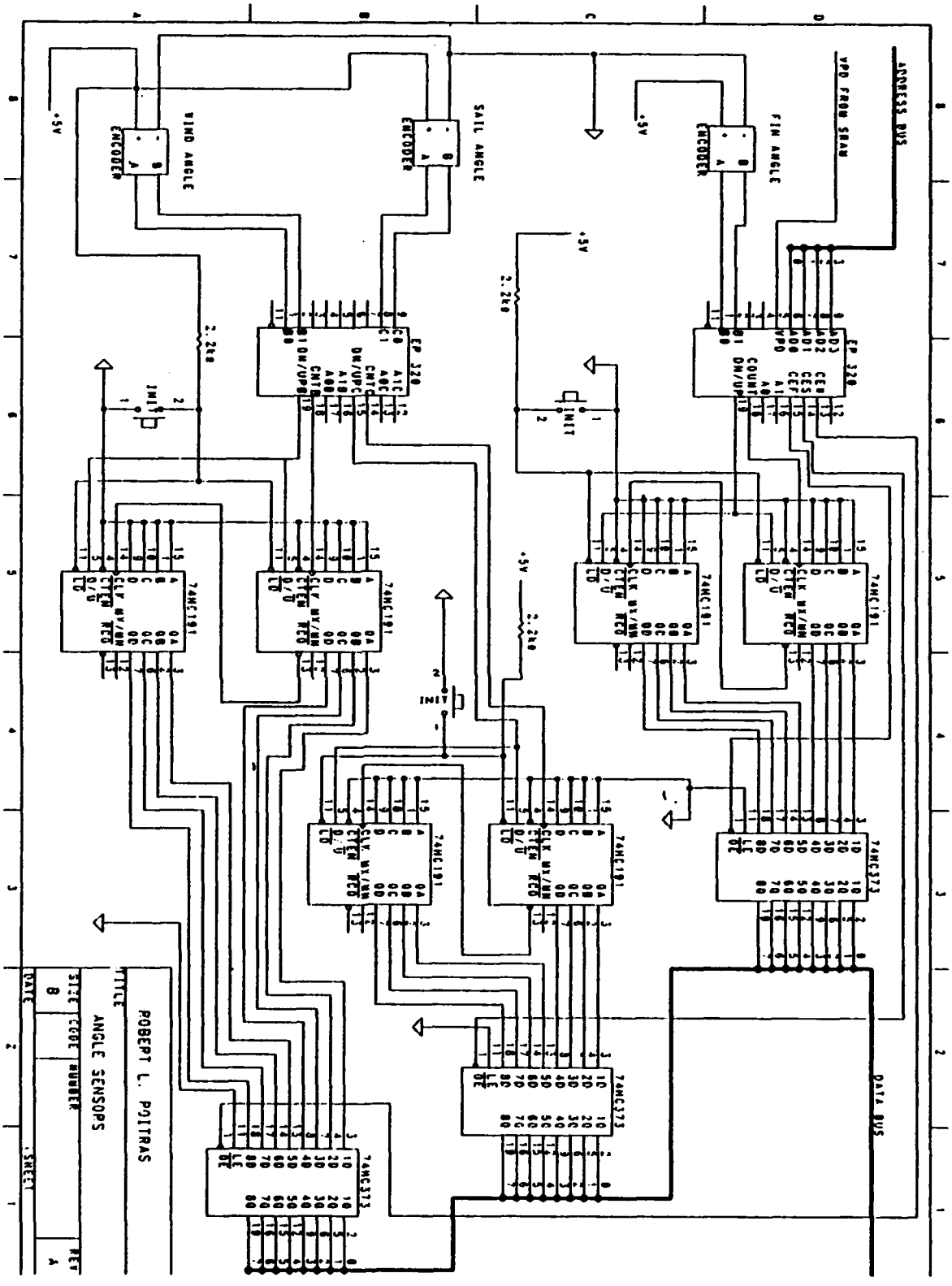
## APPENDIX B: SCHEMATIC DIAGRAMS

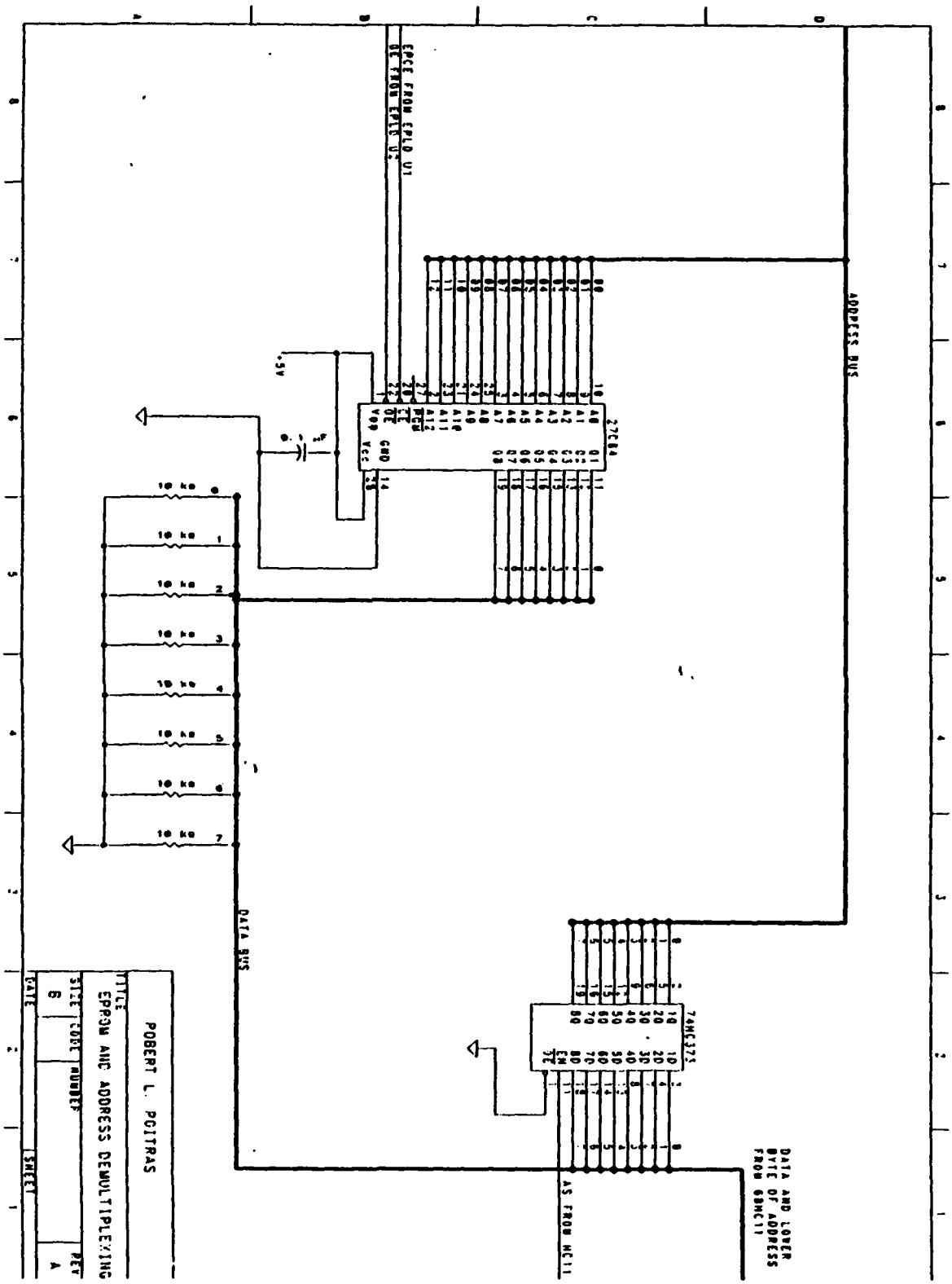
A hierarchical series of schematics follows beginning on the next page.

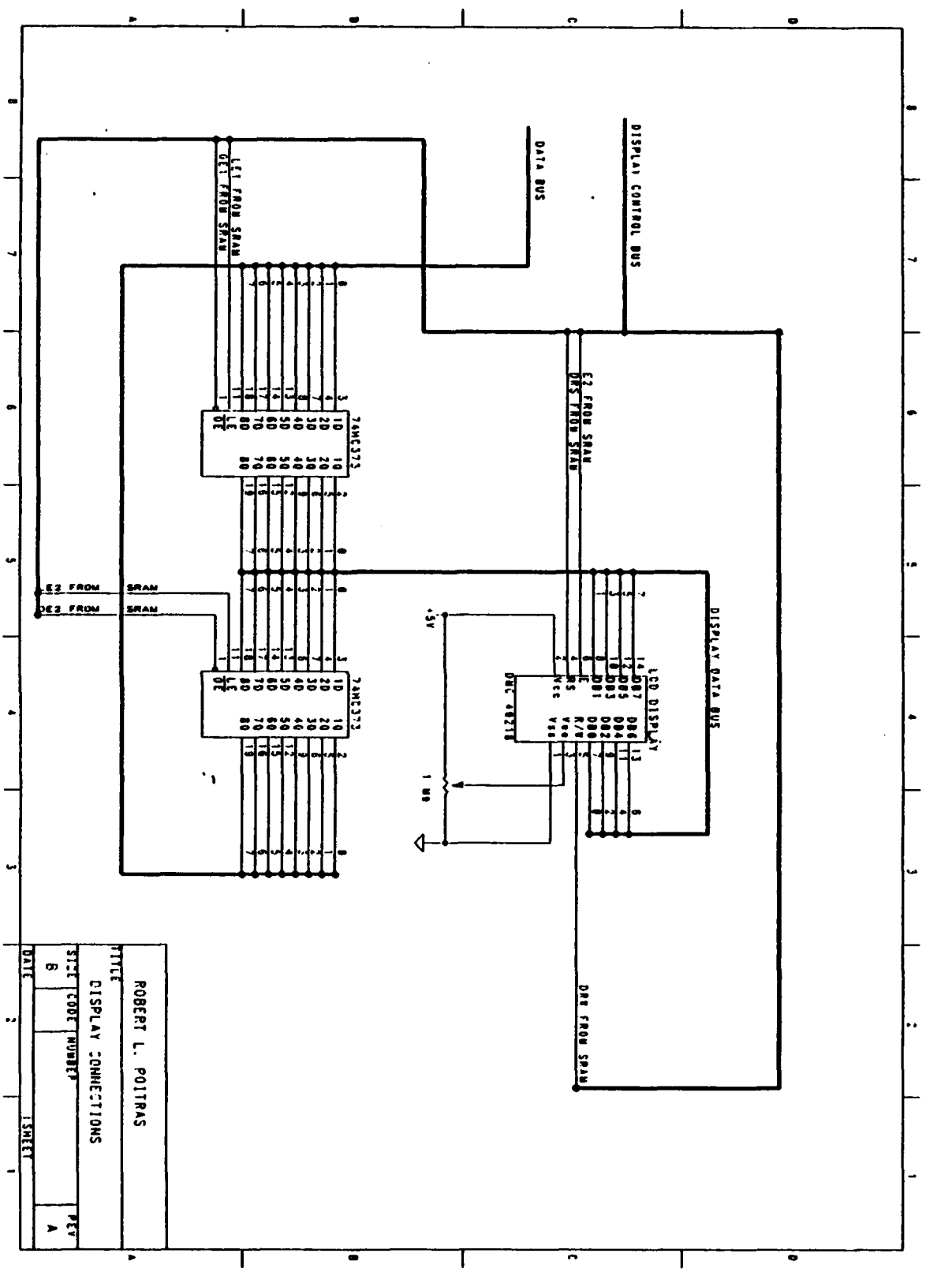

VPD
EPROM
EPCE
OE
SPAM
TO PC SERIAL PORT 9600 BAUD
NOTE THAT WILL BAUD RATE CAN BE CHANGED
TO A NUMBER OF DIFFERENT VALUES
ADDRESS BUS
DATA BUS
AS
E
R/W
RXD
TXD
COMMUNICATION
NOTE THAT THIS
CIRCUIT WILL BE
EXTERNAL TO THE
PACKAGE AND
ATTACHED AS
NEEDED FOR THE
WINDSURFING APPL.
ANGLE SENSORS
68HC11E0
WATER TEMP THERMISTOR
BOARD SPEED
WIND SPEED
DISPLAY CONTROL BUS
SPEED SENSORS
AND WATER TEMP
DISPLAY


RX FROM PORT
TX TO PORT
4.7Kø
RESET
GND
IN
MC34064
MC34164
+5V
DATA/ADDRESS 0-7
XTAL
EXTAL
R/W
E
AS
STRA/AS
MODA/LIR
MODB/VSTBY
VSS
VRH 5
VRL 5
PE7/AN75
PE3/AN34
PE6/AN64
PE2/AN24
PE1/AN14
PE0/AN04
PE4/AN44
PE5/AN54
PA0/IC3
PE7/A15
PB6/A14
PE5/A13
PB4/A12
PE3/A11
PE2/A10
PE1/A9
PB0/A8
PD0/RXD
PD1/TXD
PD2/MISO
PD3/MOSI
PD4/SCK
PD5/SS
VDD
PA7/PA1/OC1
PA6/OC2/OC1
PA5/OC3/OC1
PA4/OC4/OC1
PA3/OC5/OC1
PA2/IC1
PA1/IC2
IRQ
RESET
PC7/AD7
PC6/AD6
PC5/AD5
PC4/AD4
PC3/AD3
PC2/AD2
PC1/AD1
PC0/AD0
10kø
4.7kø
18pF
10MΩ
8MHz AT
1µF
0.01µF
FROM WINDSPEED
FROM PADDLEWHEEL
ADDRESS BUS
FROM THERMISTOR
+5v
ROBERT L. POITRAS
68HC11 INSTRUMENTATION
SIZE
CODE
NUMBER
REV
A
SHEET
DATE


DISPLAY CONTROL BUS
TO DISPLAY
E2
OR3
OR2
OE1
LE1
OE2
LE2
TO EPROM EPCE
TO EPROM OE
ADDRESS BUS
DATA BUS
PROBEFI L POITRAS
SPAM AND MEMORY DECODING


ROBERT L. POLTRAS
ANGLE SENSORS
DATA BUS
ADDRESS BUS
WIND ANGLE
SAIL ANGLE
FIN ANGLE
ENCODER
74HC191
74HC373
EP 320


ADDRESS BUS
DATA BUS
27C64
74HC373
ROBERT L. POITRAS
EPROM AND ADDRESS DEMULTIPLEXING
DATA AND LOWER BYTE OF ADDRESS FROM 68HC11
AS FROM HC11


DATA BUS
DISPLAY CONTROL BUS
CE1 FROM SRAM
CE2 FROM SRAM
OE2 FROM SRAM
WE2 FROM SRAM
74HC373
LCD DISPLAY
DISPLAY DATA BUS
ROBERT L. POITRAS
DISPLAY CONNECTIONS
SIZE
B
DATE
SHEET
REV
A

# APPENDIX C: LIST OF REGISTERS

**MC68HC11E9 Register and Control Bit Assignments (1 of 2)**

(The register block can be remapped to any 4K boundary.)

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $1000 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 | PORTA |
| $1001 | | | | | | | | | Reserved |
| $1002 | STAF | STAI | CWOM | HNDS | OIN | PLS | EGA | INVB | PIOC |
| $1003 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 | PORTC |
| $1004 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 | PORTB |
| $1005 | PCL7 | PCL6 | PCL5 | PCL4 | PCL3 | PCL2 | PCL1 | PCL0 | PORTCL |
| $1006 | | | | | | | | | Reserved |
| $1007 | DDC7 | DDC6 | DDC5 | DDC4 | DDC3 | DDC2 | DDC1 | DDC0 | DDRC |
| $1008 | 0 | 0 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 | PORTD |
| $1009 | 0 | 0 | DDD5 | DDD4 | DDD3 | DDD2 | DDD1 | DDD0 | DDRD |
| $100A | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 | PORTE |
| $100B | FOC1 | FOC2 | FOC3 | FOC4 | FOC5 | 0 | 0 | 0 | CFORC |
| $100C | OC1M7 | OC1M6 | OC1M5 | OC1M4 | OC1M3 | 0 | 0 | 0 | OC1M |
| $100D | OC1D7 | OC1D6 | OC1D5 | OC1D4 | OC1D3 | 0 | 0 | 0 | OC1D |
| $100E | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 | TCNT (High) |
| $100F | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | TCNT (Low) |
| $1010 | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 | TIC1 (High) |
| $1011 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | TIC1 (Low) |
| $1012 | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 | TIC2 (High) |
| $1013 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | TIC2 (Low) |
| $1014 | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 | TIC3 (High) |
| $1015 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | TIC3 (Low) |
| $1016 | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 | TOC1(High) |
| $1017 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | TOC1 (Low) |
| $1018 | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 | TOC2 (High) |
| $1019 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | TOC2 (Low) |
| $101A | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 | TOC3 (High) |
| $101B | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | TOC3 (Low) |
| $101C | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 | TOC4 (High) |
| $101D | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | TOC4 (Low) |
| $101E | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 | TI4O5 (High) |
| $101F | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | TI4O5 (Low) |

**MC68HC11E9 Register and Control Bit Assignments (2 of 2)**

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $1020 | OM2 | OL2 | OM3 | OL3 | OM4 | OL4 | OM5 | OL5 | TCTL1 |
| $1021 | EDG4B | EDG4A | EDG1B | EDG1A | EDG2B | EDG2A | EDG3B | EDG3A | TCTL2 |
| $1022 | OC1I | OC2I | OC3I | OC4I | I4O5I | IC1I | IC2I | IC3I | TMSK1 |
| $1023 | OC1F | OC2F | OC3F | OC4F | I4O5F | IC1F | IC2F | IC3F | TFLG1 |
| $1024 | TOI | RTII | PAOVI | PAII | 0 | 0 | PR1 | PR0 | TMSK2 |
| $1025 | TOF | RTIF | PAOVF | PAIF | 0 | 0 | 0 | 0 | TFLG2 |
| $1026 | DDRA7 | PAEN | PAMOD | PEDGE | DDRA3 | I4/O5 | RTR1 | RTR0 | PACTL |
| $1027 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | PACNT |
| $1028 | SPIE | SPE | DWOM | MSTR | CPOL | CPHA | SPR1 | SPR0 | SPCR |
| $1029 | SPIF | WCOL | 0 | MODF | 0 | 0 | 0 | 0 | SPSR |
| $102A | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | SPDR |
| $102B | TCLR | 0 | SCP1 | SCP0 | RCKB | SCR2 | SCR1 | SCR0 | BAUD |
| $102C | R8 | T8 | 0 | M | WAKE | 0 | 0 | 0 | SCCR1 |
| $102D | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK | SCCR2 |
| $102E | TDRE | TC | RDRF | IDLE | OR | NF | FE | 0 | SCSR |
| $102F | R7/T7 | R6/T6 | R5/T5 | R4/T4 | R3/T3 | R2/T2 | R1/T1 | R0/T0 | SCDR |
| $1030 | CCF | 0 | SCAN | MULT | CD | CC | CB | CA | ADCTL |
| $1031 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | ADR1 |
| $1032 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | ADR2 |
| $1033 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | ADR3 |
| $1034 | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | ADR4 |
| $1035 | 0 | 0 | 0 | PTCON | BPRT3 | BPRT2 | BPRT1 | BPRT0 | BPROT |
| $1036 to $1038 | | | | | | | | | Reserved |
| $1039 | ADPU | CSEL | IRQE | DLY | CME | 0 | CR1 | CR0 | OPTION |
| $103A | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | COPRST |
| $103B | ODD | EVEN | 0 | BYTE | ROW | ERASE | EELAT | EEPGM | PPROG |
| $103C | RBOOT | SMOD | MDA | IRVNE | PSEL3 | PSEL2 | PSEL1 | PSEL0 | HPRIO |
| $103D | RAM3 | RAM2 | RAM1 | RAM0 | REG3 | REG2 | REG1 | REG0 | INIT |
| $103E | TILOP | 0 | OCCR | CBYP | DISR | FCM | FCOP | TCON | TEST1 |
| $103F | 0 | 0 | 0 | 0 | NOSEC | NOCOP | ROMON | EEON | CONFIG |

## APPENDIX D: MEMORY MAP

| | |
|---|---|
| CONTROL REGISTERS | $0000-003F |
| 448 BYTES RAM (ON uPROCESSOR) | $0040-01FF |
| DISPLAY (READ/WRITE) | $0200 |
| DISPLAY (CONTROL) | $0201 |
| REL WIND ANGLE | $0202 |
| SAIL SHEETING ANGLE | $0203 |
| FIN ANGLE OF ATTACK | $0204 |
| RESERVED FOR EXPANSION OF SENSORS | $0205-020F |
| SRAM LOW | $0210-7FFF |
| SRAM HIGH | $8000-DFFF |
| ROM | $EOOO-FFFF |

## APPENDIX E: MEMORY EPLD DESIGN

```
MODULE MEM
TITLE 'MEMORY DECODING FOR SRAM AND EPROM
ALSO GENERATES VALID PERIPHERAL DEVICE
ROBERT L. POITRAS JAN 93'

        U1      DEVICE  'E0310';


        A15, A14, A13, A12          PIN     2,3,4,5;
        A11, A10, A9, A8            PIN     6,7,8,9;
        A7, A6 ,A5 ,A4              PIN     11,12,13,14;
        VPD                         PIN     15;
        CSRL                        PIN     16;
        CSRH                        PIN     17;
        EPCE                        PIN     18;
        OR7654                      PIN     19;
        OR7654                      ISTYPE  'POS,COM,FEED_OR';
        A6, A5,A4                   ISTYPE  'FEED_PIN';
        H,L,X       =       1,0,.X.;
        ADDRESS     =       [A15,A14,A13,A12,A11,A10,A9,A8,A7,A6,A5,A4,X,X,X,X];

EQUATIONS
        VPD   = !A15&!A14&!A13&!A12&!A11&!A10&A9&!A8&!A7&!A6&!A5&!A4;
      !CSRL   = (!A15& !A14& !A13& !A12& OR7654& A9) #
                (!A15& !A14& !A13& !A12& OR7654& A10) #
                (!A15& !A14& !A13& !A12& OR7654& A11);
       CSRH   = (!A15&!A14&!A13&!A12)#(A15&A14&A13);
      !EPCE   = (A15&A14&A13);
       OR7654= (A7# A6# A5# A4);

TEST_VECTORS     (ADDRESS->[OR7654, EPCE, CSRH, CSRL, VPD])
                 ^h0200   ->[ L,    H,    H,    H,    H ];
                 ^h020F   ->[ L,    H,    H,    H,    H ];
                 ^h0210   ->[ H,    H,    H,    L,    L ];
                 ^h0FFF   ->[ H,    H,    H,    L,    L ];
                 ^h1000   ->[ L,    H,    L,    H,    L ];
                 ^hDFFF   ->[ H,    H,    L,    H,    L ];
                 ^hE000   ->[ L,    L,    H,    H,    L ];
                 ^hFFFF   ->[ H,    L,    H,    H,    L ];
                 ^h01FF   ->[ H,    H,    H,    H,    L ];


END MEM
```

```
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MEMORY DECODING FOR SRAM AND EPROM
ALSO GENERATES VALID PERIPHERAL DEVICE
ROBERT L. POITRAS JAN 93
Equations for Module MEM

Device U1


- Reduced Equations:

    VPD = (!A10 & !A11 & !A12 & !A13 & !A14 & !A15 & !A4 & !A5 & !A6 & !A7
         & !A8 & A9);

    CSRL = !(A11 & !A12 & !A13 & !A14 & !A15 & OR7654
            # A10 & !A12 & !A13 & !A14 & !A15 & OR7654
            # !A12 & !A13 & !A14 & !A15 & A9 & OR7654);


    CSRH = (A13 & A14 & A15 # !A12 & !A13 & !A14 & !A15);

    EPCE = !(A13 & A14 & A15);

    OR7654 = (A4 # A5 # A6 # A7);
```

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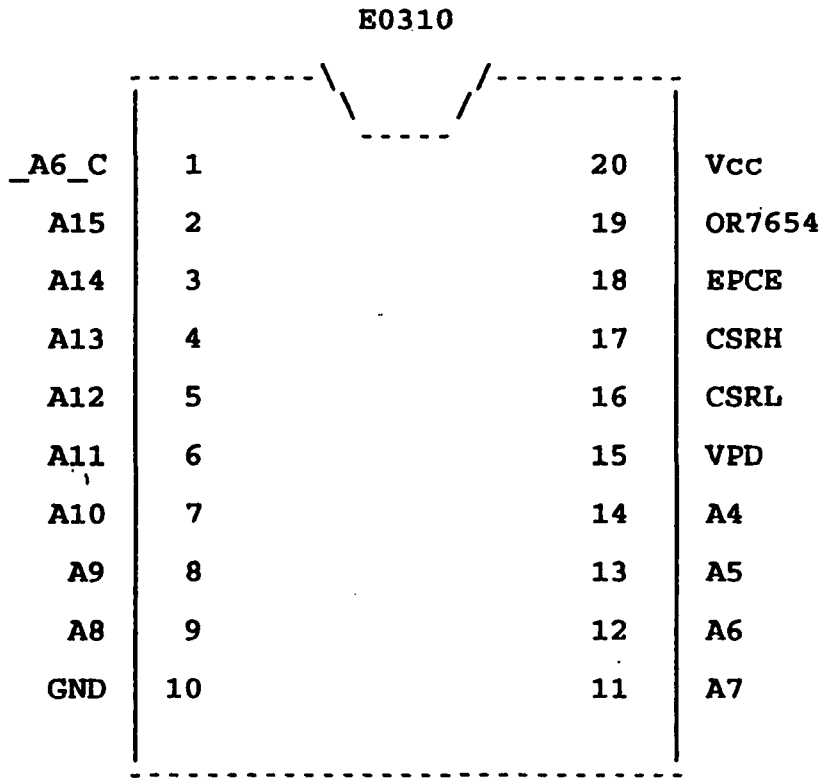
MEMORY DECODING FOR SRAM AND EPROM
ALSO GENERATES VALID PERIPHERAL DEVICE
ROBERT L. POITRAS JAN 93
Chip diagram for Module MEM

Device U1




end of module MEM

# APPENDIX F: DMC 40218 LCD DISPLAY INSTRUCTIONS

| Instruction | Code | | | | | | | | | | Description | Execution time (max) (when fcp or fosc is 250kHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Clears entire display and sets DD RAM address 0 in address counter. | 1.64ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | • | Sets DD RAM address 0 is address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged. | 1.64ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor move direction and specifies shift of display. These operations are performed during data write and read. | 40μs |
| Display ON/OFF Control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B). | 40μs |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | • | • | Moves cursor and shifts display without changing DD RAM contents. | 40μs |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | • | • | Sets interface data length (DL), number of display lines (L) and character font (F). | 40μs |
| Set CG RAM Address | 0 | 0 | 0 | 1 | AGC | | | | | | Sets CG RAM address. CG RAM data is sent and received after this setting. | 40μs |
| Set DD RAM Address | 0 | 0 | 1 | ADD | | | | | | | Sets DD RAM address. DD RAM data is sent and received after this setting. | 40μs |
| Read Busy Flag & Address | 0 | 1 | BF | AC | | | | | | | Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents. | 40μs |
| Write Data to CG or DD RAM | 1 | 0 | Write Date | | | | | | | | Writes data into DD RAM or CG RAM. | 40μs |
| Read Data from CG or DD RAM | 1 | 1 | Read Data | | | | | | | | Reads data from DD RAM or CG RAM. | 40μs |
| | I/D=1 : Increment<br>I/D=0 : Decrement<br>S=1 : Accompanies display shift.<br>S/C=1 : Display shift<br>S/C=0 : Cursor move<br>R/L=1 : Shift to the right.<br>R/L=0 : Shifts to the left.<br>DL=1 : 8 bits, DL=0 : 4 bits.<br>N=1 : 2 lines, N=0: 1 line<br>F=1 : 5x10 dots, F=0: 5x7 dots<br>BF=1 : Internally operating<br>BF=0 : Can accept instruction | | | | | | | | | | DD RAM : Display data RAM<br>CG RAM : Character generator RAM<br>ACC : CG RAM address<br>ADD : DD RAM address. Corresponds to cursor address.<br>AC : Address counter used for both DD and CG RAM address. | Execution time changes when frequency changes. (Example) When fcp or fosc is 270kHz:<br>$40\mu s \times \frac{250}{270} = 37\mu s$ |

* No Effect

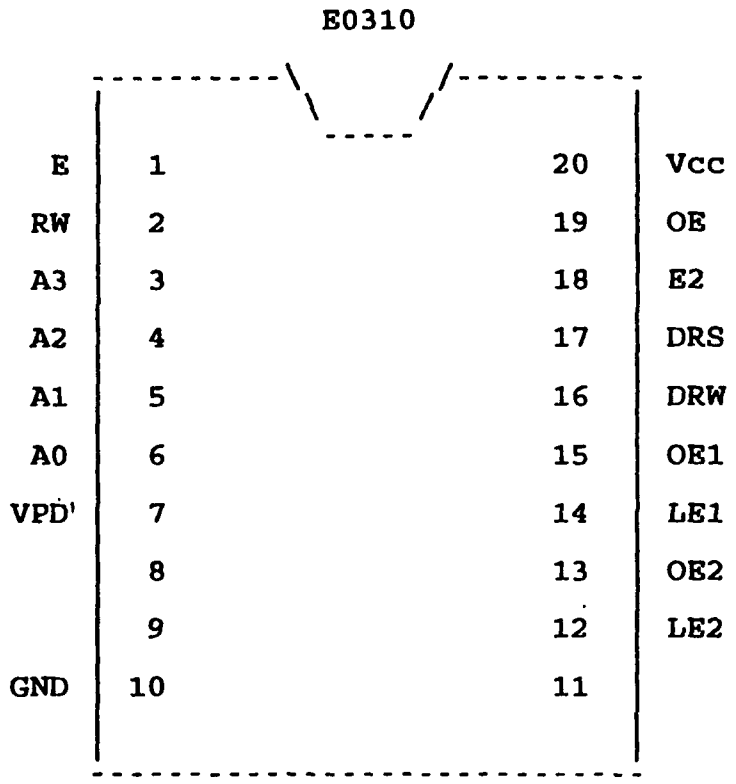
## APPENDIX G: DISPLAY EPLD DESIGN

```
MODULE DISPLAY
TITLE 'LOGIC TO DRIVE THE DMC40218 LCD DISPLAY
ROBERT L. POITRAS JAN 93'

        U2      DEVICE  'E0310';

        E               PIN     1;
        RW              PIN     2;
        A3,A2,A1,A0     PIN     3,4,5,6;
        VPD             PIN     7;
        LE2,OE2         PIN     12,13;
        LE1,OE1         PIN     14,15;
        DRW             PIN     16;
        DRS             PIN     17;
        E2              PIN     18;
        E2              ISTYPE  'POS, REG, FEED_REG';
        OE              PIN     19;
        H,L,X           =       1,0,.X.;
        ADDRESS         =       [A3, A2,A1, A0];

EQUATIONS
        LE2 = VPD& !A3& !A2& !A1& RW;
        !OE2= (VPD& !A3& !A2& !A1& RW);
        LE1 = VPD& !A3& !A2& !A1& !RW;
        !OE1= (!VPD# A3# A2# A1# !RW);
        DRW = VPD& !A3& !A2& !A1& RW;
        DRS = VPD& !A3& !A2& !A1& !A0;
        E2  := !E2;
        !OE = (E& RW);

TEST_VECTORS    ([ADDRESS, VPD, RW]->[DRS, DRW, OE1, LE1, OE2, LE2])
                [^h0,       H,   H]->[ H,    H,   H,   L,   L,   H ];
                [^h0,       H,   L]->[ H,    L,   L,   H,   H,   L ];
                [^h1,       H,   H]->[ L,    H,   H,   L,   L,   H ];
                [^h1,       H,   L]->[ L,    L,   L,   H,   H,   L ];
                [^h1,       L,   L]->[ L,    L,   L,   L,   H,   L ];

TEST_VECTORS    ([E, E2, RW]->[ OE,  E2])
                 [0, 0,   1]->[ H,   L];
                 [1, 0,   1]->[ L,   H];
                 [0, 1,   0]->[ H,   H];
                 [1, 1,   0]->[ H,   L];

END DISPLAY
```

```
ABEL(tm) 3.00a  -  Document Generator                    21-Jan-93 03:39 PM
LOGIC TO DRIVE THE DMC40218 LCD DISPLAY
ROBERT L. POITRAS JAN 93
Equations for Module DISPLAY

Device U2


- Reduced Equations:

    LE2 = (!A1 & !A2 & !A3 & RW & VPD);

    OE2 = !(!A1 & !A2 & !A3 & RW & VPD);

    LE1 = (!A1 & !A2 & !A3 & !RW & VPD);

    OE1 = !(!RW # A1 # A2 # A3 # !VPD);

    DRW = (!A1 & !A2 & !A3 & RW & VPD);

    DRS = (!A0 & !A1 & !A2 & !A3 & VPD);

    E2 := (!E2);

    OE = !(E & RW);
```

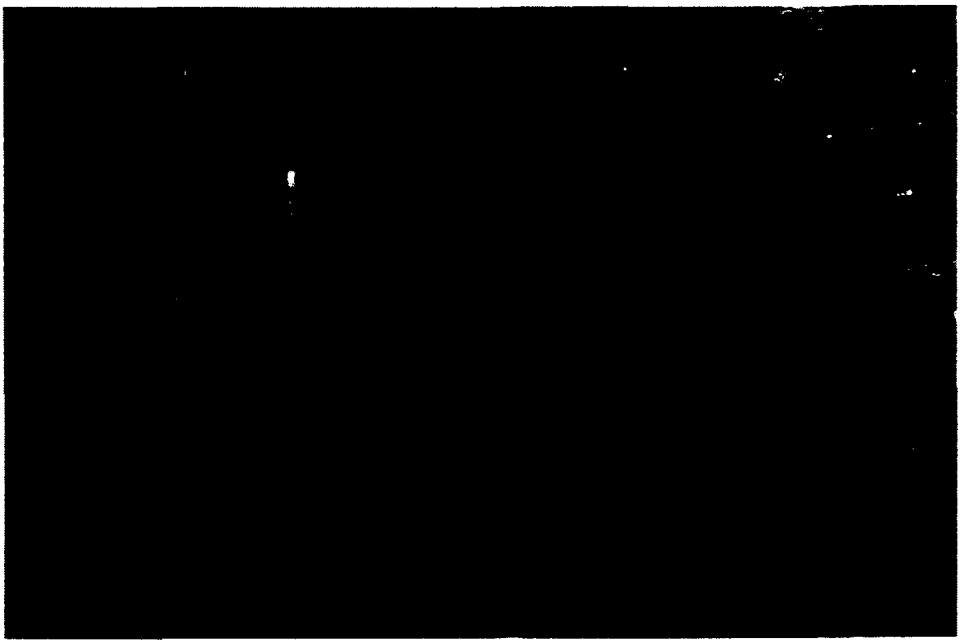
ABEL(tm) 3.00a - Document Generator 21-Jan-93 03:39 PM
LOGIC TO DRIVE THE DMC40218 LCD DISPLAY
ROBERT L. POITRAS JAN 93
Chip diagram for Module DISPLAY

Device U2

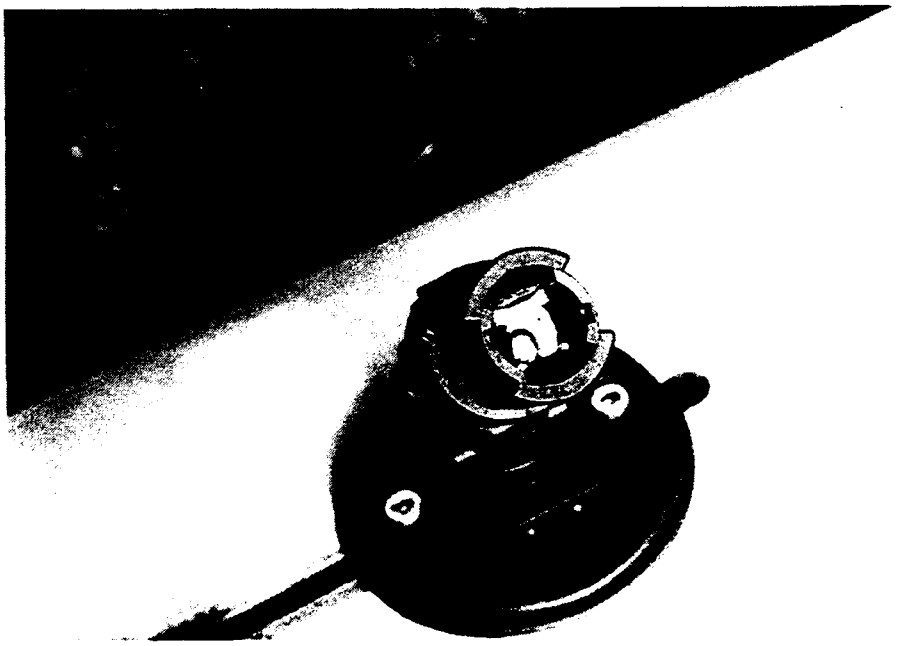



end of module DISPLAY

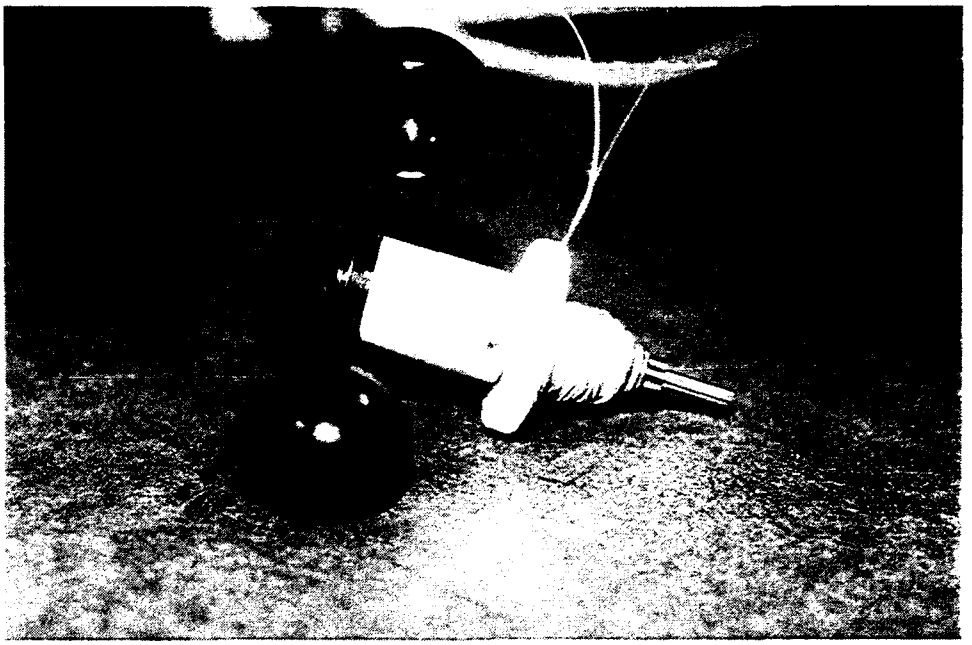
## APPENDIX H: SENSOR PHOTOGRAPHS



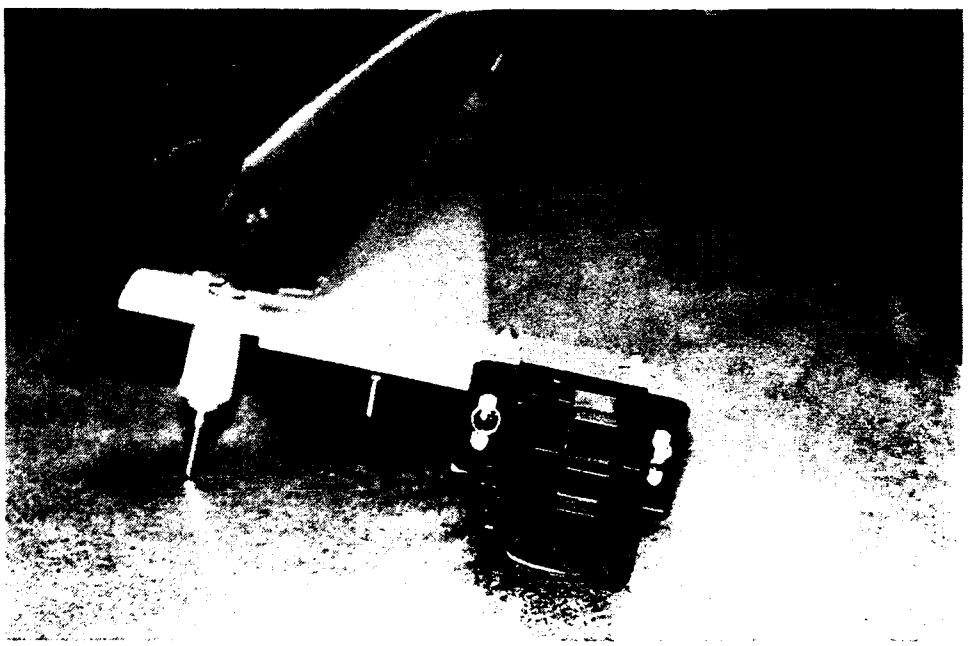
Water Resistant Encoder Chamber and Seal



Sail Sheeting Angle Encoder Mounted in Mast Extension Adapter Cup



Windspeed Sensor



Boardspeed Sensor and Trailing Fin on T-Bar Mount

Sensors Mounted On Windsurfing Craft

## APPENDIX I: SINGLE FSM DESIGN

MODULE FSM

```
TITLE 'A FSM TO TAKE IN THE TWO BIT GRAY CODE OF
AN OPTICAL ENCODER AND DRIVE THE DN_UP AND CLK
INPUTS TO A 74HC191 BINARY UP/DOWN COUNTER.
ROBERT L. POITRAS FEB 93'

        U3      DEVICE  'E0320';

        B0, B1          PIN     1,2;
        DN_UP           PIN     19;
        COUNT           PIN     18;
        A0,A1           PIN     17,16;

        DN_UP, COUNT    ISTYPE  'POS, COM, FEED_OR';
        A0, A1          ISTYPE  'POS, COM, FEED_OR';

        H,L,X           =       1,0,.X.;
        GIN             =       [B1, B0];

EQUATIONS
        A1 = (B1& A1) # (A1& COUNT) # (A1& B0 & !DN_UP) # (A1& !B0& DN_UP)
             # (!A0& B1& !COUNT) # (A0& B1& !DN_UP& !COUNT);

        A0 = (A0& B0) # (A0& COUNT) # (!A1& B0& !DN_UP& !COUNT) #
             (A0& !B1& !DN_UP) # (A1& B0& DN_UP& !COUNT) #
             (A0& B1& DN_UP);

        DN_UP = (DN_UP& COUNT) # (!A1& !B0& DN_UP) # (A0& B1& DN_UP) #
             (A1& B0& DN_UP) # (A1& !A0& B1& DN_UP) #
             (A1& !A0& B1& B0& !COUNT) # (!A1& A0& !B1& !B0& !COUNT)
             # (A1& A0& !B1& B0& !COUNT);

        COUNT = (!A1& !A0& !B1& !B0) # (A1& !A0& !B1& B0) # (A1& A0& B1& B0)
             # (A1& !A0& B1& !B0);

TEST_VECTORS    ([GIN] -> [A1, A0,DN_UP, COUNT])
                [^h0 ] -> [L,  L,   L,      L];
                [^h1 ] -> [L,  H,   L,      L];
                [^h2 ] -> [H,  H,   L,      L];
                [^h1 ] -> [L,  H,   L,      L];

END FSM
```

```
ABEL(tm) 3.00a  -  Document Generator                    23-Feb-93 08:21 PM
A FSM TO TAKE IN THE TWO BIT GRAY CODE OF
AN OPTICAL ENCODER AND DRIVE THE DN_UP AND CLK
INPUTS TO A 74HC191 BINARY UP/DOWN COUNTER.
ROBERT L. POITRAS FEB 93
Equations for Module FSM

Device U3


- Reduced Equations:

    A1 = (A0 & B1 & !COUNT & !DN_UP
          # !A0 & B1 & !COUNT
          # A1 & !B0 & DN_UP
          # A1 & B0 & !DN_UP
          # A1 & COUNT
          # A1 & B1);


    A0 = (A0 & B1 & DN_UP
          # A1 & B0 & !COUNT & DN_UP
          # A0 & !B1 & !DN_UP
          # !A1 & B0 & !COUNT & !DN_UP
          # A0 & COUNT
          # A0 & B0);


    DN_UP = (A0 & A1 & B0 & !B1 & !COUNT
             # A0 & !A1 & !B0 & !B1 & !COUNT
             # !A0 & A1 & B0 & B1 & !COUNT
             # !A0 & A1 & B1 & DN_UP
             # A1 & B0 & DN_UP
             # A0 & B1 & DN_UP
             # !A1 & !B0 & DN_UP
             # COUNT & DN_UP);


    COUNT = (!A0 & A1 & !B0 & B1
             # A0 & A1 & B0 & B1
             # !A0 & A1 & B0 & !B1
             # !A0 & !A1 & !B0 & !B1);
```

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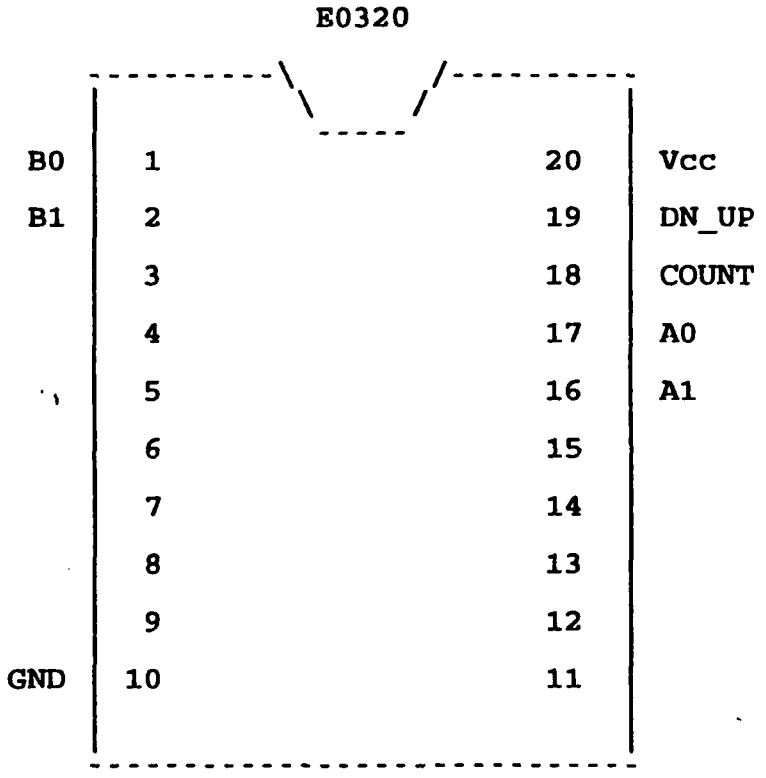
A FSM TO TAKE IN THE TWO BIT GRAY CODE OF
AN OPTICAL ENCODER AND DRIVE THE DN_UP AND CLK
INPUTS TO A 74HC191 BINARY UP/DOWN COUNTER.
ROBERT L. POITRAS FEB 93
Chip diagram for Module FSM

Device U3



# APPENDIX J: DOUBLE FSM DESIGN

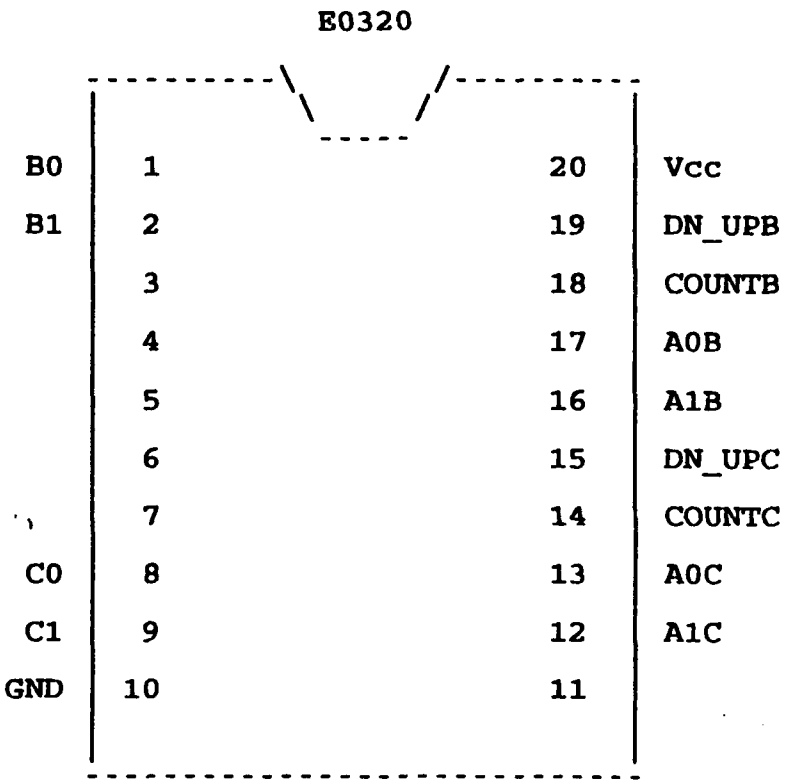
```
                MODULE FSM2

TITLE 'A FSM TO TAKE IN THE TWO BIT GRAY CODE OF
TWO OPTICAL ENCODERS AND DRIVE THE DN_UP AND CLK
INPUTS TO A 74HC191 BINARY UP/DOWN COUNTER FOR
EACH ENCODER.
ROBERT L. POITRAS FEB 93'

        U4      DEVICE  'E0320';

        B0, B1          PIN     1,2;
        C0, C1          PIN     8,9;
        DN_UPB          PIN     19;
        DN_UPC          PIN     15;
        COUNTB          PIN     18;
        COUNTC          PIN     14;
        A0B,A1B         PIN     17,16;
        A0C,A1C         PIN     13,12;

        DN_UPB, COUNTB    ISTYPE  'POS, COM, FEED_OR';
        A0B, A1B          ISTYPE  'POS, COM, FEED_OR';
        DN_UPC, COUNTC    ISTYPE  'POS, COM, FEED_OR';
        A0C, A1C          ISTYPE  'POS, COM, FEED_OR';
        H,L,X           =       1,0,.X.;
        GIN             =       [B1, B0];

EQUATIONS
        A1B = (B1& A1B) # (A1B& COUNTB) # (A1B& B0 & !DN_UPB) # (A1B& !B0& DN_UP
              # (!A0B& B1& !COUNTB) # (A0B& B1& !DN_UPB& !COUNTB);

        A0B = (A0B& B0) # (A0B& COUNTB) # (!A1B& B0& !DN_UPB& !COUNTB) #
              (A0B& !B1& !DN_UPB) # (A1B& B0& DN_UPB& !COUNTB) #
              (A0B& B1& DN_UPB);

        DN_UPB = (DN_UPB& COUNTB) # (!A1B& !B0& DN_UPB) # (A0B& B1& DN_UPB) #
              (A1B& B0& DN_UPB) # (A1B& !A0B& B1& DN_UPB) #
              (A1B& !A0B& B1& B0& !COUNTB) # (!A1B& A0B& !B1& !B0& !COUNTB)
              # (A1B& A0B& !B1& B0& !COUNTB);

        COUNTB = (!A1B& !A0B& !B1& !B0) # (A1B& !A0B& !B1& B0) # (A1B& A0B& B1&
              # (A1B& !A0B& B1& !B0);

        A1C = (C1& A1C) # (A1C& COUNTC) # (A1C& C0 & !DN_UPC) # (A1C& !C0& DN_UP
              # (!A0C& C1& !COUNTC) # (A0C& C1& !DN_UPC& !COUNTC);

        A0C = (A0C& C0) # (A0C& COUNTC) # (!A1C& C0& !DN_UPC& !COUNTC) #
              (A0C& !C1& !DN_UPC) # (A1C& C0& DN_UPC& !COUNTC) #
              (A0C& C1& DN_UPC);

        DN_UPC = (DN_UPC& COUNTC) # (!A1C& !C0& DN_UPC) # (A0C& C1& DN_UPC) #
              (A1C& C0& DN_UPC) # (A1C& !A0C& C1& DN_UPC) #
              (A1C& !A0C& C1& C0& !COUNTC) # (!A1C& A0C& !C1& !C0& !COUNTC)
              # (A1C& A0C& !C1& C0& !COUNTC);

        COUNTC = (!A1C& !A0C& !C1& !C0) # (A1C& !A0C& !C1& C0) # (A1C& A0C& C1&
              # (A1C& !A0C& C1& !C0);

END FSM2
```

```
ABEL(tm) 3.00a  -  Document Generator                    24-Feb-93 09:59 AM
A FSM TO TAKE IN THE TWO BIT GRAY CODE OF
TWO OPTICAL ENCODERS AND DRIVE THE DN_UP AND CLK
INPUTS TO A 74HC191 BINARY UP/DOWN COUNTER FOR
EACH ENCODER.
ROBERT L. POITRAS FEB 93
Equations for Module FSM2

Device U4


- Reduced Equations:

    A1B = (A0B & B1 & !COUNTB & !DN_UPB
           # !A0B & B1 & !COUNTB
           # A1B & !B0 & DN_UPB
           # A1B & B0 & !DN_UPB
           # A1B & COUNTB
           # A1B & B1);


    A0B = (A0B & B1 & DN_UPB
           # A1B & B0 & !COUNTB & DN_UPB
           # A0B & !B1 & !DN_UPB
           # !A1B & B0 & !COUNTB & !DN_UPB
           # A0B & COUNTB
           # A0B & B0);


    DN_UPB = (A0B & A1B & B0 & !B1 & !COUNTB
              # A0B & !A1B & !B0 & !B1 & !COUNTB
              # !A0B & A1B & B0 & B1 & !COUNTB
              # !A0B & A1B & B1 & DN_UPB
              # A1B & B0 & DN_UPB
              # A0B & B1 & DN_UPB
              # !A1B & !B0 & DN_UPB
              # COUNTB & DN_UPB);


    COUNTB = (!A0B & A1B & !B0 & B1
              # A0B & A1B & B0 & B1
              # !A0B & A1B & B0 & !B1
              # !A0B & !A1B & !B0 & !B1);


    A1C = (A0C & C1 & !COUNTC & !DN_UPC
           # !A0C & C1 & !COUNTC
           # A1C & !C0 & DN_UPC
           # A1C & C0 & !DN_UPC
           # A1C & COUNTC
           # A1C & C1);


    A0C = (A0C & C1 & DN_UPC
           # A1C & C0 & !COUNTC & DN_UPC
           # A0C & !C1 & !DN_UPC
           # !A1C & C0 & !COUNTC & !DN_UPC
```

```
ABEL(tm) 3.00a  -  Document Generator                    24-Feb-93 09:59 AM
A FSM TO TAKE IN THE TWO BIT GRAY CODE OF
TWO OPTICAL ENCODERS AND DRIVE THE DN_UP AND CLK
INPUTS TO A 74HC191 BINARY UP/DOWN COUNTER FOR
EACH ENCODER.
ROBERT L. POITRAS FEB 93
Equations for Module FSM2

Device U4

            # A0C & COUNTC
            # A0C & C0);


    DN_UPC = (A0C & A1C & C0 & !C1 & !COUNTC
              # A0C & !A1C & !C0 & !C1 & !COUNTC
              # !A0C & A1C & C0 & C1 & !COUNTC
              # !A0C & A1C & C1 & DN_UPC
              # A1C & C0 & DN_UPC
              # A0C & C1 & DN_UPC
              # !A1C & !C0 & DN_UPC
              # COUNTC & DN_UPC);


    COUNTC = (!A0C & A1C & !C0 & C1
              # A0C & A1C & C0 & C1
              # !A0C & A1C & C0 & !C1
              # !A0C & !A1C & !C0 & !C1);
```

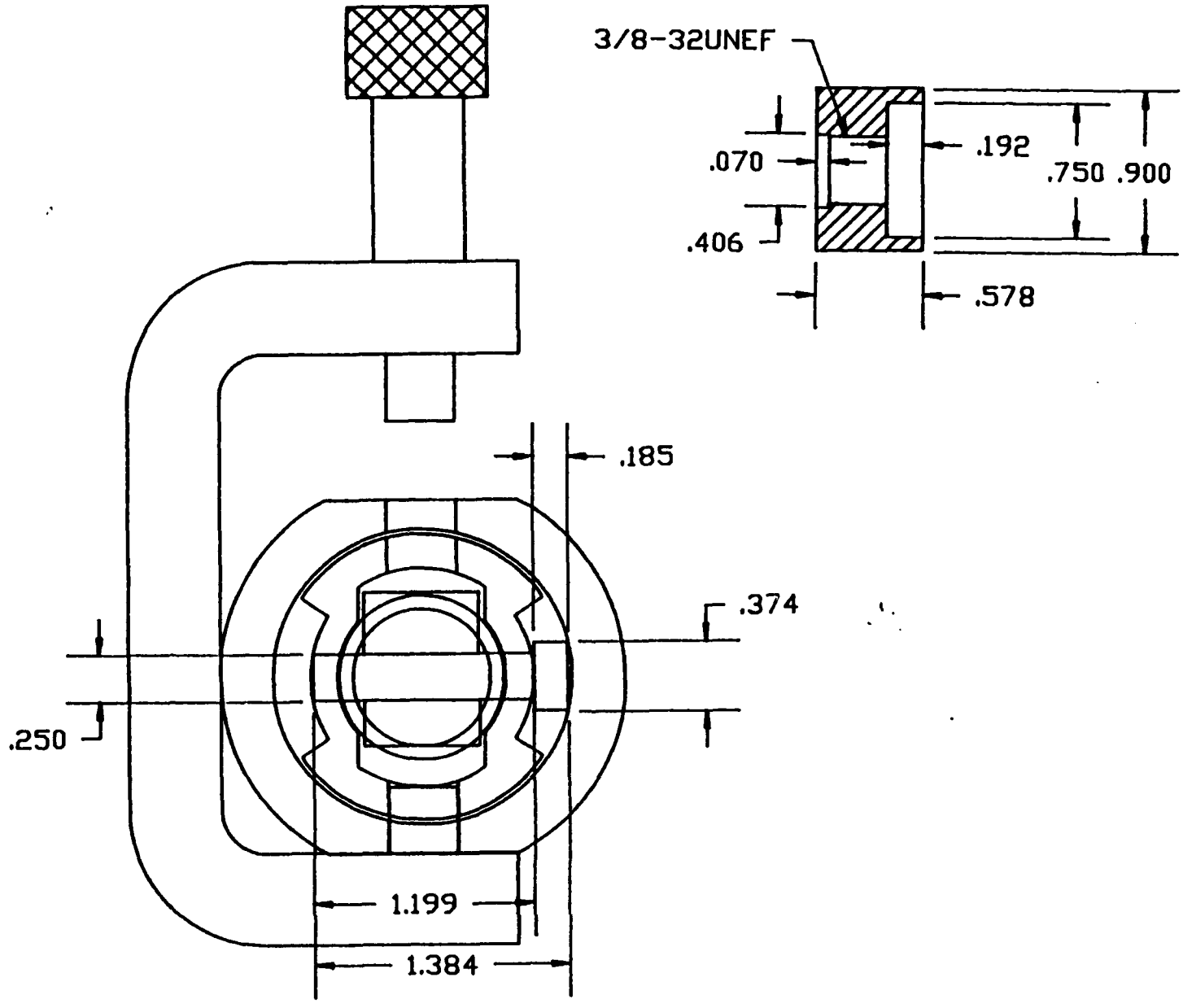
ABEL(tm) 3.00a - Document Generator 24-Feb-93 09:59 AM
A FSM TO TAKE IN THE TWO BIT GRAY CODE OF
TWO OPTICAL ENCODERS AND DRIVE THE DN_UP AND CLK
INPUTS TO A 74HC191 BINARY UP/DOWN COUNTER FOR
EACH ENCODER.
ROBERT L. POITRAS FEB 93
Chip diagram for Module FSM2

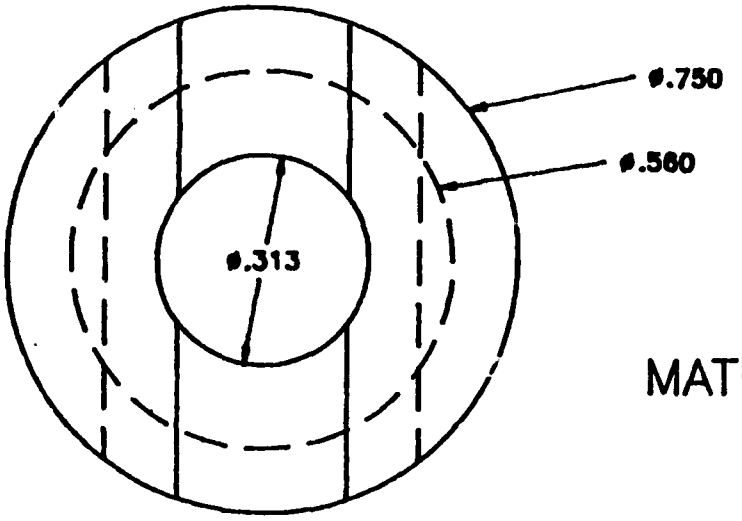
Device U4



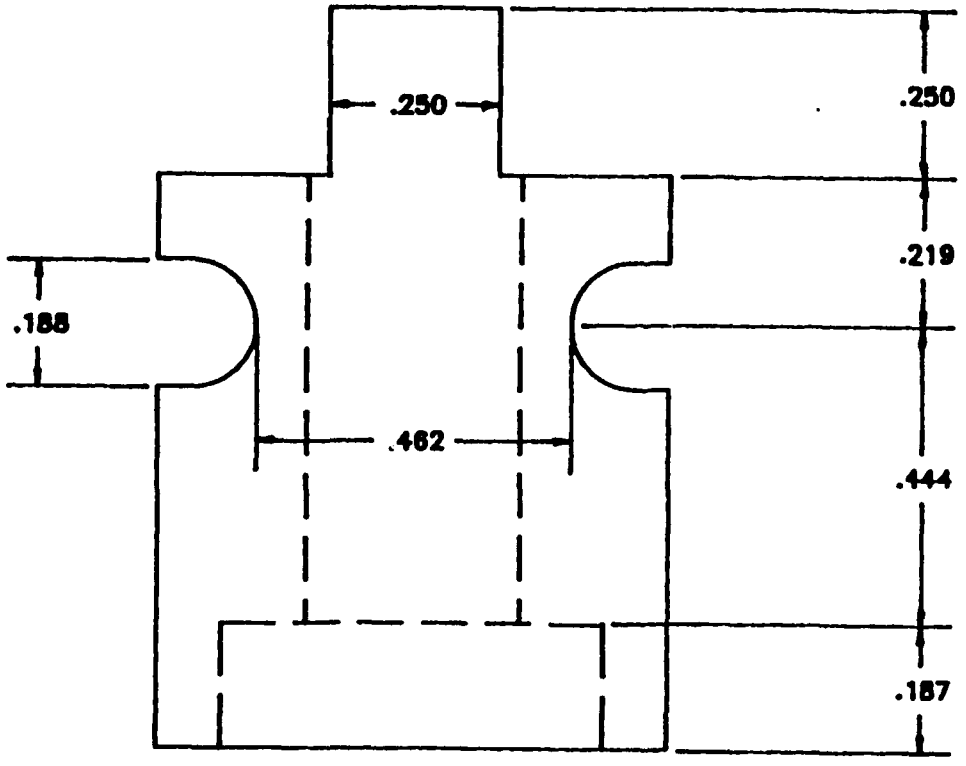

end of module FSM2

## APPENDIX K: ENCODER INTERFACE COMPONENTS

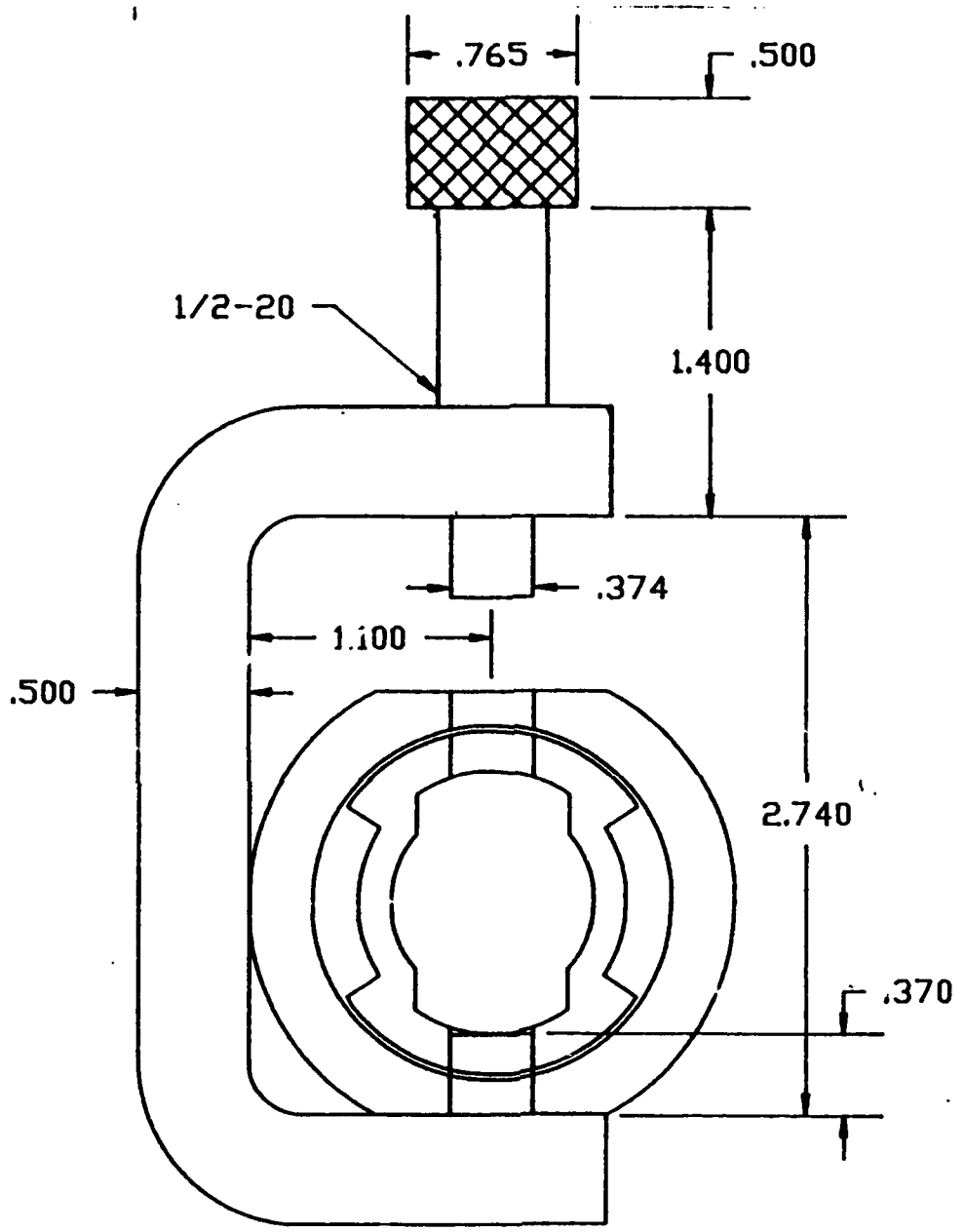





MATERIAL:BRASS




SPUD

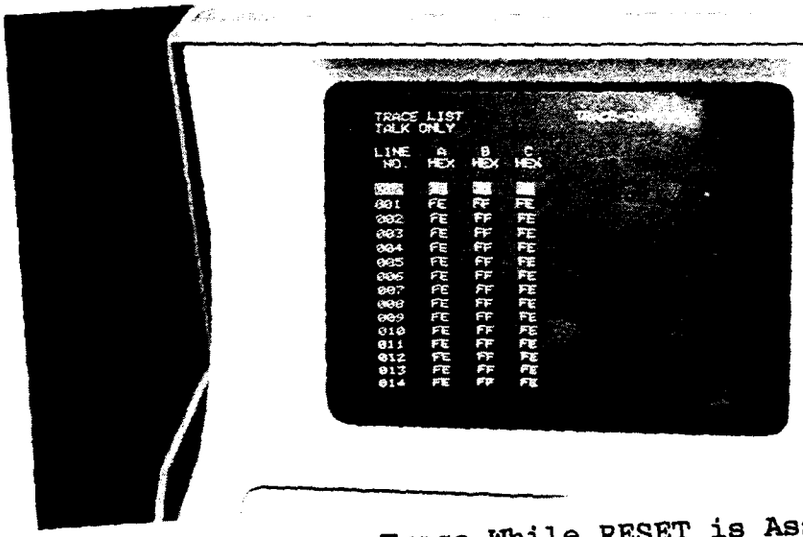

.765
.500
1/2-20
1.400
.374
1.100
.500
2.740
.370

## APPENDIX L: HELLO PROGRAM

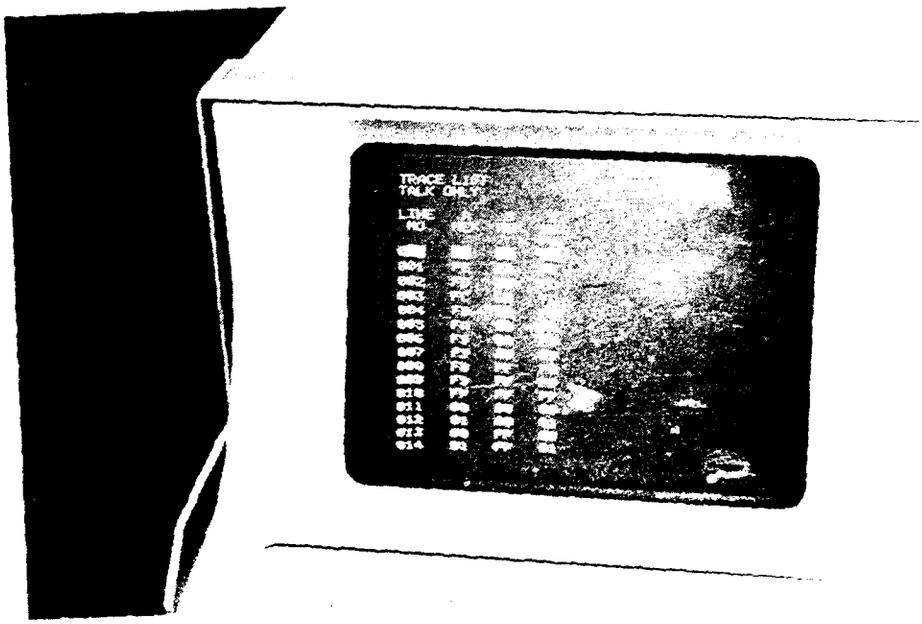
```
;*************************************************************
;*                        DISPLAY                            *
;*       THIS IS A SIMPLE TEST PROGRAM TO MAKE THE DMC       *
;*       40218 DISPLAY SAY HELLO.  I AM READING THE          *
;*       BUSY BIT FROM THE DISPLAY IN THIS TEST.             *
;*                                                           *
;*                                                           *
;*                ROBERT L. POITRAS  JAN 93                  *
;*************************************************************

        .EQU    DISCON,H'0201       ;*use this label for control
        .EQU    DISWRT,H'0200       ;*USE THIS LABEL FOR DATA
        .EQU    DISRDY,H'80

        .ORG    H'E000

INITIAL LDS     #H'01FA             ;*INITIALIZES THE STACK

HELLO   LDAA    #H'38
        STAA    DISCON              ;*DISPLAY FUNCTION SET
        BSR     TILCLR

        LDAA    #H'01               ;*DISPLAY CLEAR
        STAA    DISCON
        BSR     TILCLR

        LDAA    #H'07
        STAA    DISCON              ;*SETS ENTRY MODE
        BSR     TILCLR

        LDAA    #H'0E
        STAA    DISCON              ;*SETS DISPLAY ON WITH CURSOR AND BLINK
        BSR     TILCLR

        LDAA    #'H'
        STAA    DISWRT              ;* WRITES CHARACTER 'H' TO DISPLAY
        BSR     TILCLR

        LDAA    #'E'
        STAA    DISWRT              ;* WRITES 'E'
        BSR     TILCLR

        LDAA    #'L'                ;* WRITES 'L'
        STAA    DISWRT
        BSR     TILCLR

        LDAA    #'L'
        STAA    DISWRT              ;* WRITES 'L'
        BSR     TILCLR
```

```
        LDAA    #'O'
        STAA    DISWRT          ;* WRITES 'O'
        BSR     TILCLR
        STOP

;*  THIS ENDS THE MAIN PROGRAM

;* THIS IS THE SUBROUTINE THAT CHECKS IF THE DISPLAY IS CLEAR

TILCLR  LDAA    DISCON

DLOOP   CMPA    #DISRDY

        BLT     DLOOP
        RTS

;*  THIS ENDS THE DELAY SUBROUTINE

;* THIS IS INCLUDED TO AS A REMINDER TO
;* SET THE RESET VECTOR IN THE EPROM
;* AT THE HIGHEST MEMORY LOCATION

        .ORG    H'FFFE
RESET   .DW     H'E000          ;*SETS THE POR/EXTERNAL RESET VECTOR

;*THE END
```

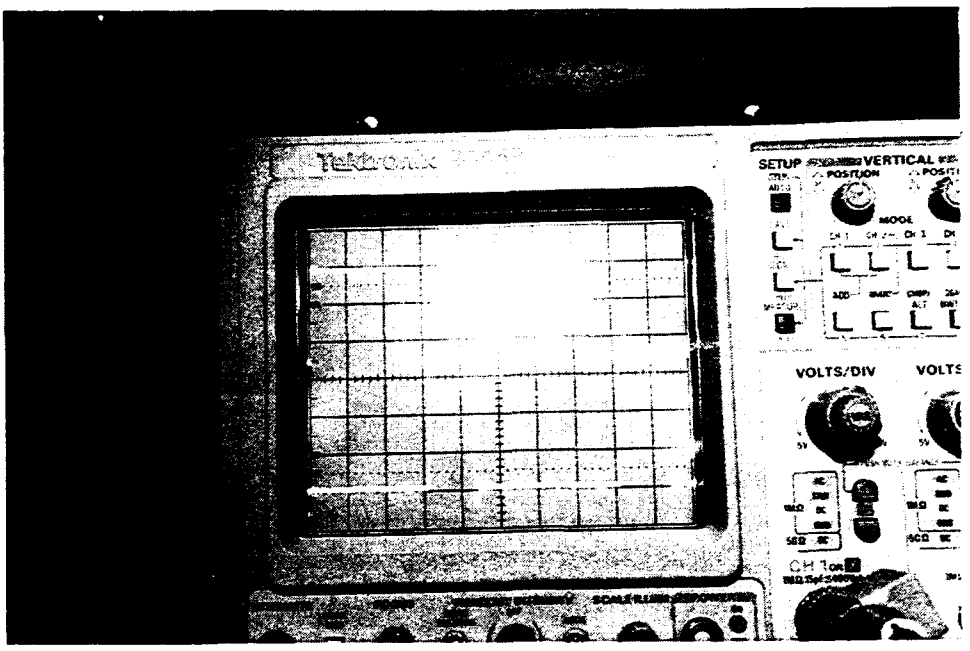
## APPENDIX M: TROUBLESHOOTING TRACES



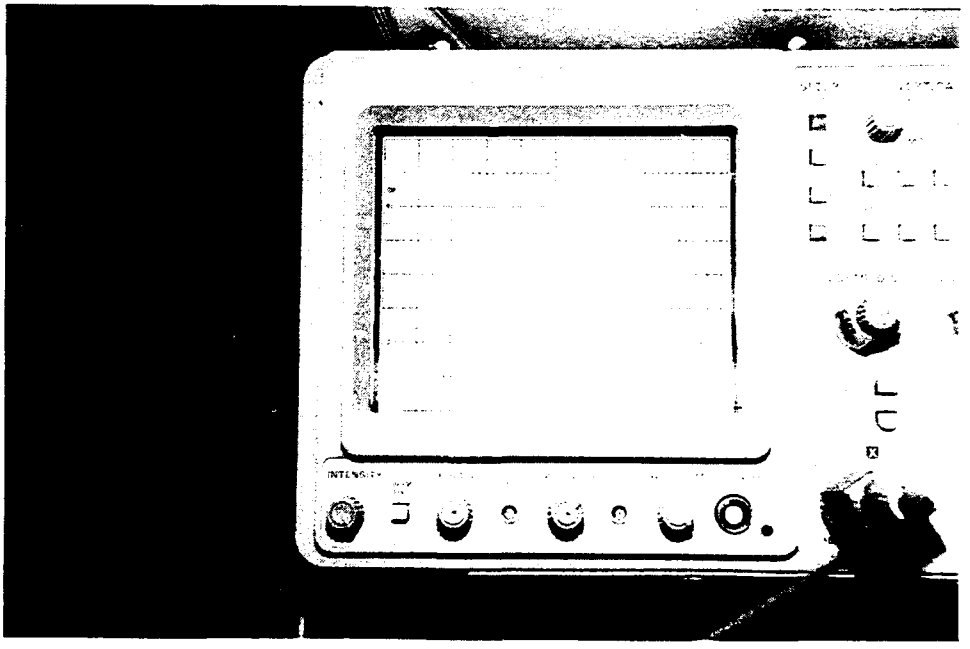

Logic Analyzer Trace While RESET is Asserted (note A-data bus, B-upper address byte, C-lower address byte. Lower address byte not registered to analyzer due to multiplexing of address and data.)



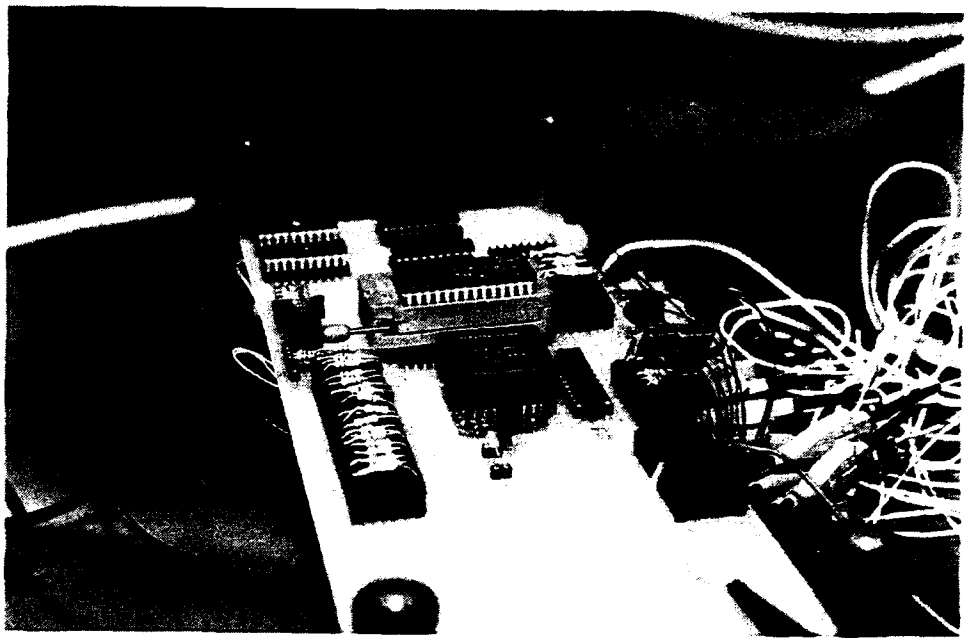
Logic Analyzer Trace During Start of Execution



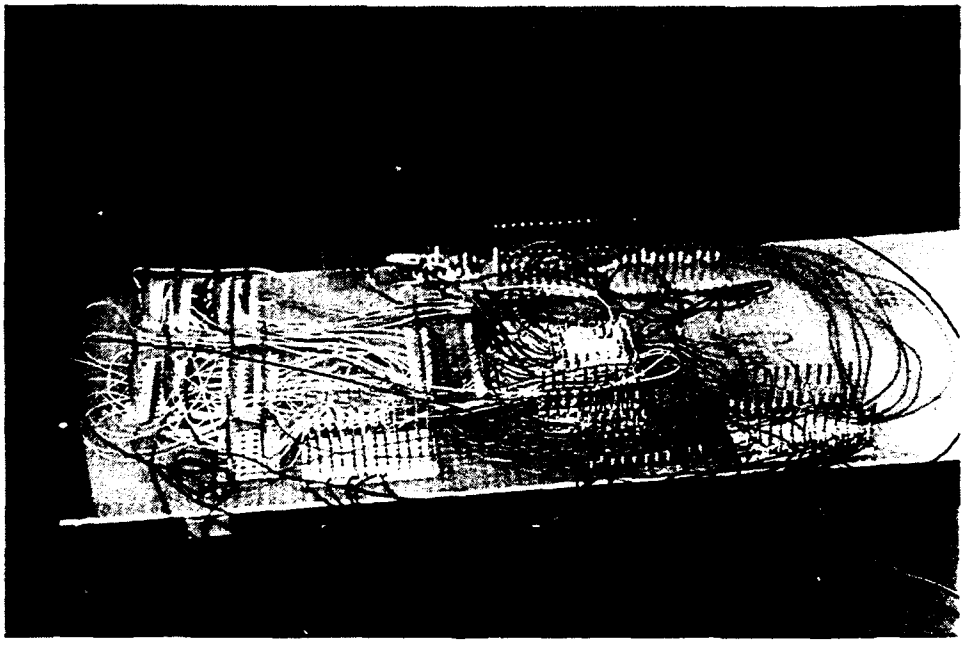

68HC11E0 E Clock Output (Top Trace)
68HC11E0 AS Output (Bottom Trace)



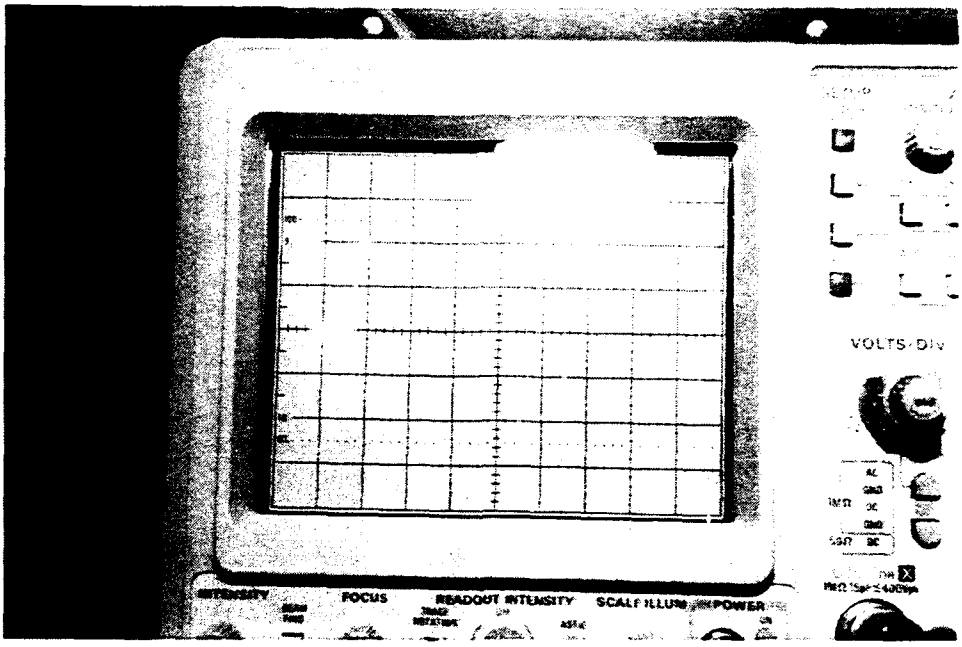
HC11E0 E clock (Top Trace)
Clock Supplied to Display (Lower Trace)



Top and Bottom Views of the Wire Wrap Prototype As Tested

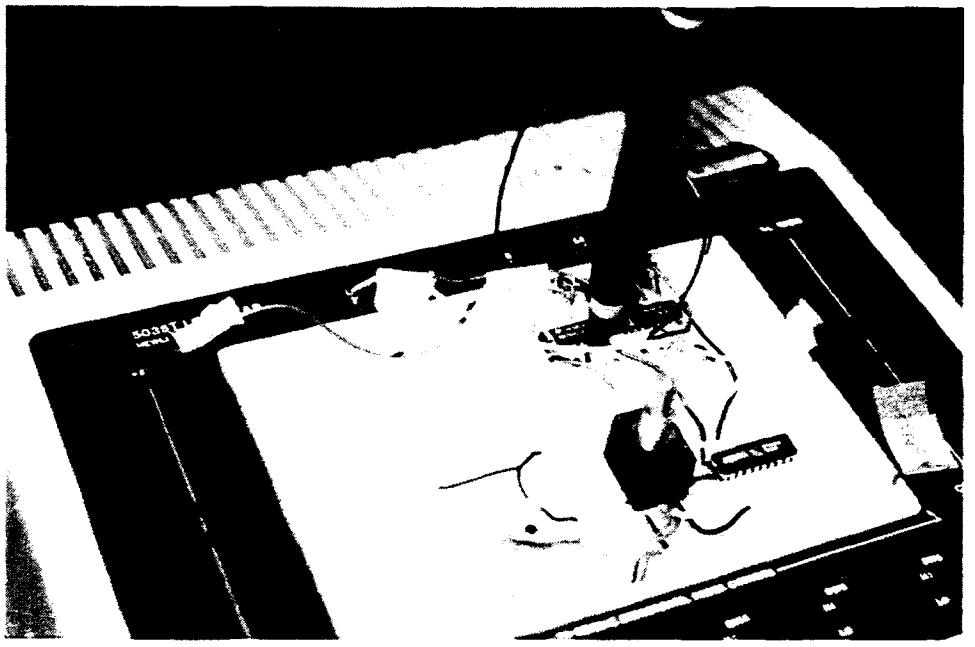


## APPENDIX N: PADDLEWHEEL TRANSDUCER WAVEFORMS




Waveform of the Board Speed Transducer

## APPENDIX O: ENCODER TESTING



This photograph shows the testing apparatus used to verify correct operation of the FSM and counter circuits.

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